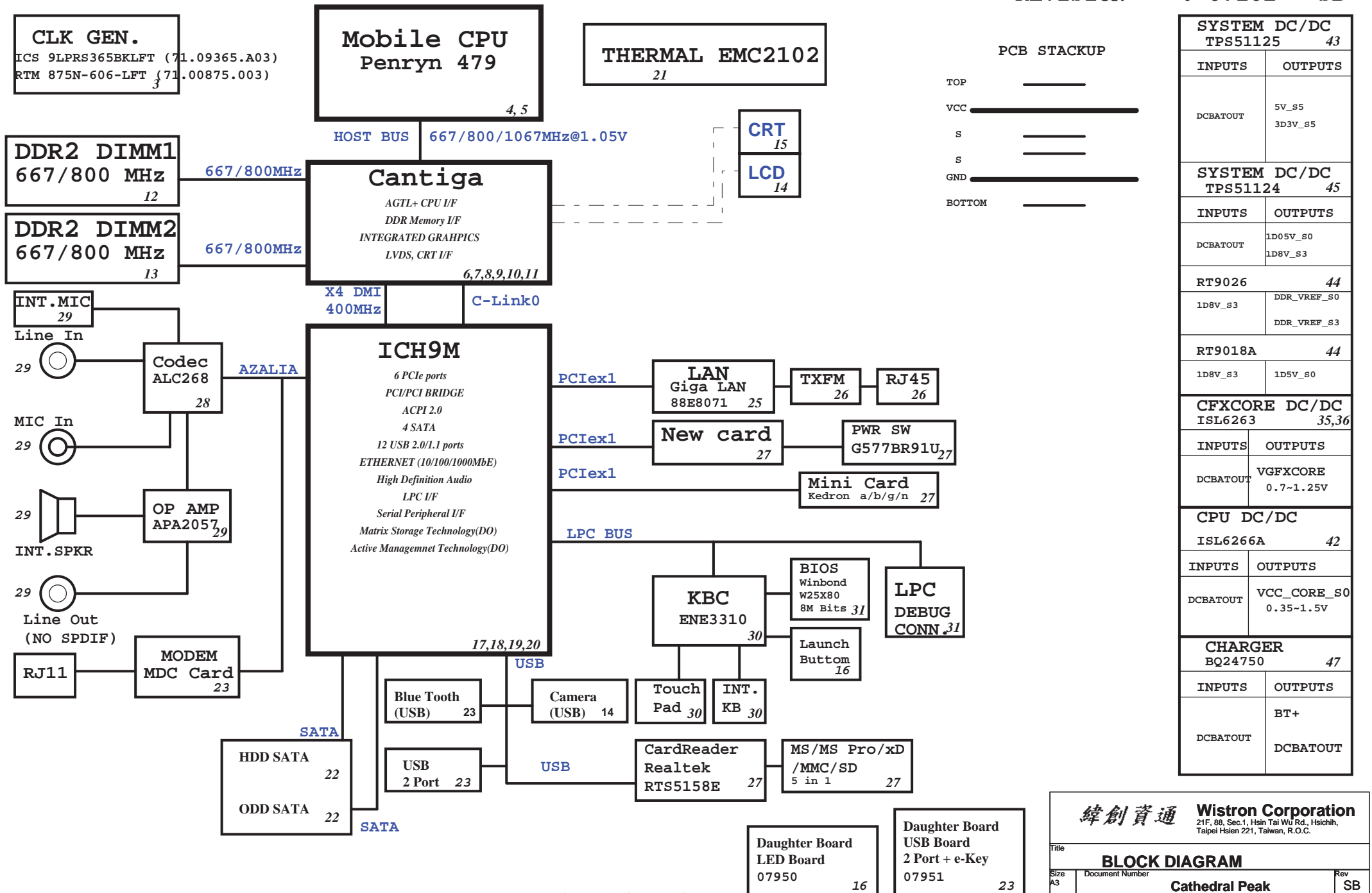


Cathedral Peak Block Diagram

Project code: 91.4J501.001
PCB P/N : 48.4J501.001
REVISION : 07261 - SB



<http://hobi-elektronika.net>

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BLOCK DIAGRAM		
Title	Document Number	Rev
Size A3	Cathedral Peak	SB
Date: Tuesday, February 12, 2008	Sheet 1 of 42	

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

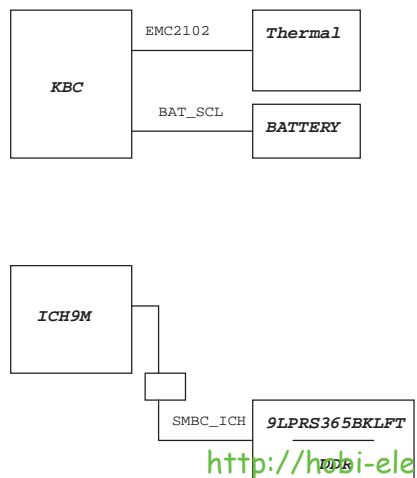
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NewCard
LANE6	NC

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	NC
4	USB3
5	Bluetooth
6	NC
7	MINIC1
8	WEBCAM
9	NEW1
10	Card Reader
11	NC

SMBus



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS1PVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN. GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled(Note2) 1 = The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

緯創資通

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Title

Reference

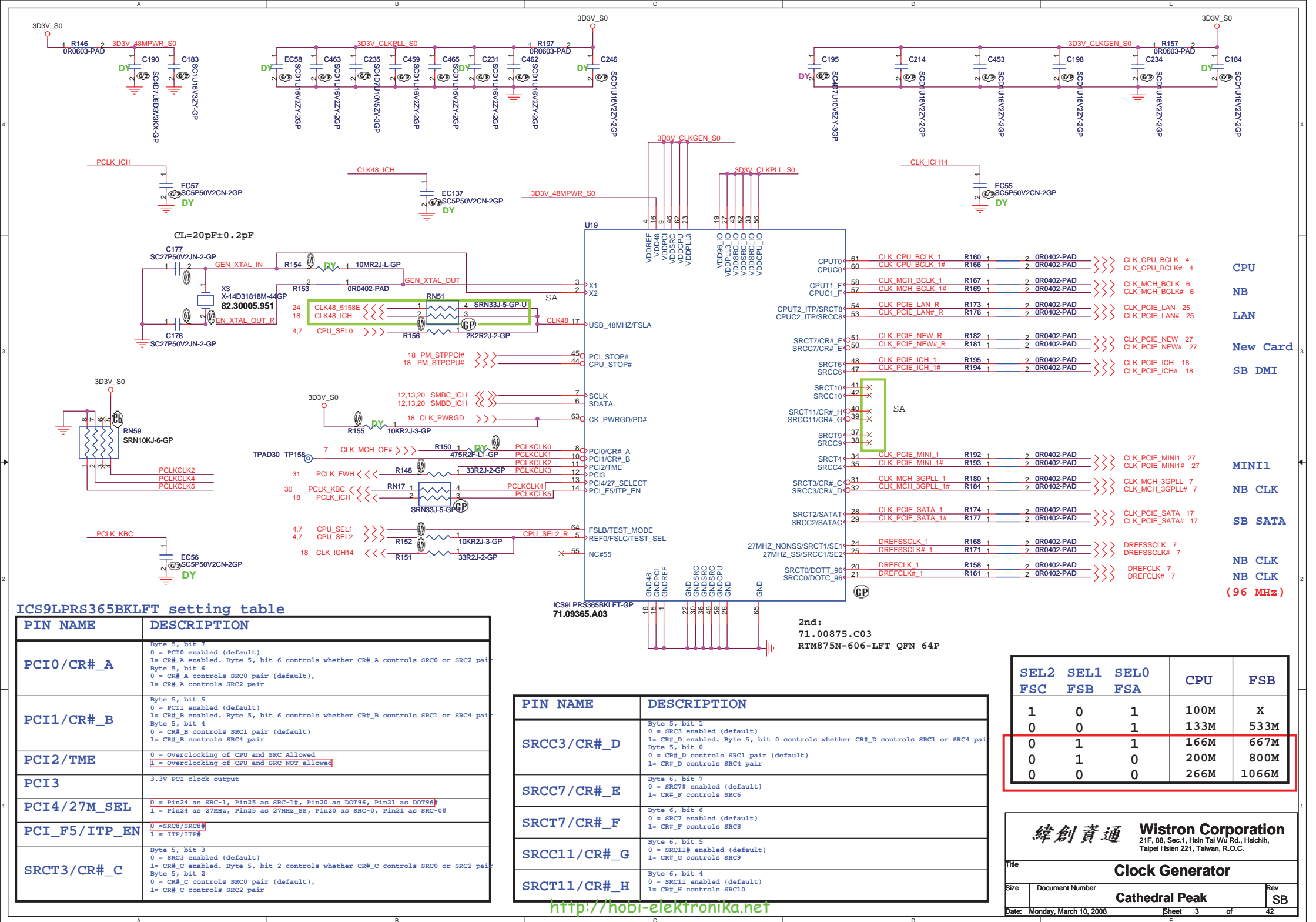
Size A3

Document Number

Date: Monday, March 10, 2008

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Rev SB



6 H_A#(35..3) <<>> H_A#(35..3)

6 H_ADSTB#0 <<>> H_REQ#(4..0)

Side Band
Non GTL

6 H_ADSTB#1 <<>> H_A#(35..3)

17 H_A20M# <<>> H_A#(35..3)

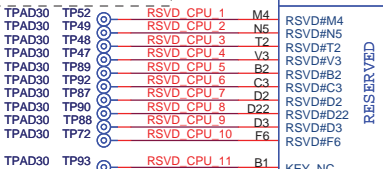
17 H_FERR# <<>> H_A#(35..3)

17 H_STPCLK# <<>> H_A#(35..3)

17 H_INTR <<>> H_A#(35..3)

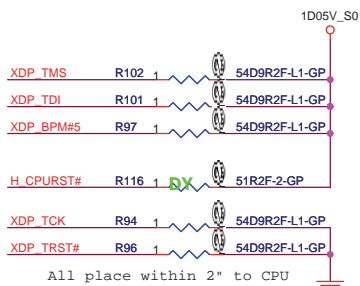
17 H_NMI <<>> H_A#(35..3)

17 H_SM# <<>> H_A#(35..3)



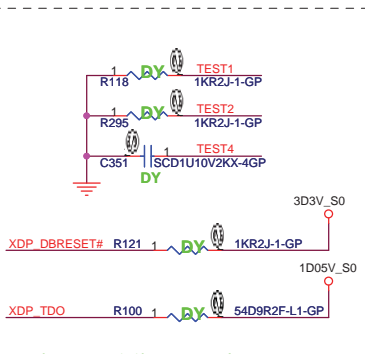
BGA479-SKT6-GPU6
62.10079.001

2nd: 62.10053.401



All place within 2" to CPU

Follow Demo Circuit



Net "TEST4" as short as possible,
make sure "TEST4" routing is
reference to GND and away other
noisy signals

H_DINV#(3..0) <<>> H_DINV#(3..0) 6
H_DSTBN#(3..0) <<>> H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<>> H_DSTBP#(3..0) 6
H_D#(63..0) <<>> H_D#(63..0) 6

6 H_D#0 E22# D0# H_D#32
6 H_D#1 E22# D1# H_D#33
6 H_D#2 E22# D2# H_D#34
6 H_D#3 G22# D3# H_D#35
6 H_D#4 F22# D4# H_D#36
6 H_D#5 G22# D5# H_D#37
6 H_D#6 E22# D6# H_D#38
6 H_D#7 E22# D7# H_D#39
6 H_D#8 K22# D8# H_D#40
6 H_D#9 G22# D9# H_D#41
6 H_D#10 J22# D10# H_D#42
6 H_D#11 J22# D11# H_D#43
6 H_D#12 H22# D12# H_D#44
6 H_D#13 F22# D13# H_D#45
6 H_D#14 K22# D14# H_D#46
6 H_D#15 H22# D15# H_D#47

6 H_DSTBN#0 <<>> H_DSTBN#0 6
6 H_DSTBP#0 <<>> H_DSTBP#0 6
6 H_DINV#0 <<>> H_DINV#0 6

6 H_D#16 N22# D16# H_D#48
6 H_D#17 K22# D17# H_D#49
6 H_D#18 P22# D18# H_D#50
6 H_D#19 R22# D19# H_D#51
6 H_D#20 L22# D20# H_D#52
6 H_D#21 M22# D21# H_D#53
6 H_D#22 L22# D22# H_D#54
6 H_D#23 M22# D23# H_D#55
6 H_D#24 P22# D24# H_D#56
6 H_D#25 P22# D25# H_D#57
6 H_D#26 P22# D26# H_D#58
6 H_D#27 T22# D27# H_D#59
6 H_D#28 R22# D28# H_D#60
6 H_D#29 L22# D29# H_D#61
6 H_D#30 T22# D30# H_D#62
6 H_D#31 N22# D31# H_D#63

6 H_DSTBN#1 <<>> H_DSTBN#1 6
6 H_DSTBP#1 <<>> H_DSTBP#1 6
6 H_DINV#1 <<>> H_DINV#1 6

6 H_D#32 E22# D32# H_D#64
6 H_D#33 F22# D33# H_D#65
6 H_D#34 G22# D34# H_D#66
6 H_D#35 H22# D35# H_D#67
6 H_D#36 I22# D36# H_D#68
6 H_D#37 J22# D37# H_D#69
6 H_D#38 K22# D38# H_D#70
6 H_D#39 L22# D39# H_D#71
6 H_D#40 M22# D40# H_D#72
6 H_D#41 N22# D41# H_D#73
6 H_D#42 O22# D42# H_D#74
6 H_D#43 P22# D43# H_D#75
6 H_D#44 Q22# D44# H_D#76
6 H_D#45 R22# D45# H_D#77
6 H_D#46 S22# D46# H_D#78
6 H_D#47 T22# D47# H_D#79

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#2 <<>> H_DSTBN#2 6
6 H_DSTBP#2 <<>> H_DSTBP#2 6
6 H_DINV#2 <<>> H_DINV#2 6

6 H_D#48 E22# D48# H_D#80
6 H_D#49 F22# D49# H_D#81
6 H_D#50 G22# D50# H_D#82
6 H_D#51 H22# D51# H_D#83
6 H_D#52 I22# D52# H_D#84
6 H_D#53 J22# D53# H_D#85
6 H_D#54 K22# D54# H_D#86
6 H_D#55 L22# D55# H_D#87
6 H_D#56 M22# D56# H_D#88
6 H_D#57 N22# D57# H_D#89
6 H_D#58 O22# D58# H_D#90
6 H_D#59 P22# D59# H_D#91
6 H_D#60 Q22# D60# H_D#92
6 H_D#61 R22# D61# H_D#93
6 H_D#62 S22# D62# H_D#94
6 H_D#63 T22# D63# H_D#95

6 H_DSTBN#3 <<>> H_DSTBN#3 6
6 H_DSTBP#3 <<>> H_DSTBP#3 6
6 H_DINV#3 <<>> H_DINV#3 6

6 H_D#64 E22# D64# H_D#96
6 H_D#65 F22# D65# H_D#97
6 H_D#66 G22# D66# H_D#98
6 H_D#67 H22# D67# H_D#99
6 H_D#68 I22# D68# H_D#100
6 H_D#69 J22# D69# H_D#101
6 H_D#70 K22# D70# H_D#102
6 H_D#71 L22# D71# H_D#103
6 H_D#72 M22# D72# H_D#104
6 H_D#73 N22# D73# H_D#105
6 H_D#74 O22# D74# H_D#106
6 H_D#75 P22# D75# H_D#107
6 H_D#76 Q22# D76# H_D#108
6 H_D#77 R22# D77# H_D#109
6 H_D#78 S22# D78# H_D#110
6 H_D#79 T22# D79# H_D#111

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#4 <<>> H_DSTBN#4 6
6 H_DSTBP#4 <<>> H_DSTBP#4 6
6 H_DINV#4 <<>> H_DINV#4 6

6 H_D#80 E22# D80# H_D#112
6 H_D#81 F22# D81# H_D#113
6 H_D#82 G22# D82# H_D#114
6 H_D#83 H22# D83# H_D#115
6 H_D#84 I22# D84# H_D#116
6 H_D#85 J22# D85# H_D#117
6 H_D#86 K22# D86# H_D#118
6 H_D#87 L22# D87# H_D#119
6 H_D#88 M22# D88# H_D#120
6 H_D#89 N22# D89# H_D#121
6 H_D#90 O22# D90# H_D#122
6 H_D#91 P22# D91# H_D#123
6 H_D#92 Q22# D92# H_D#124
6 H_D#93 R22# D93# H_D#125
6 H_D#94 S22# D94# H_D#126
6 H_D#95 T22# D95# H_D#127

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#5 <<>> H_DSTBN#5 6
6 H_DSTBP#5 <<>> H_DSTBP#5 6
6 H_DINV#5 <<>> H_DINV#5 6

6 H_D#112 E22# D112# H_D#128
6 H_D#113 F22# D113# H_D#129
6 H_D#114 G22# D114# H_D#130
6 H_D#115 H22# D115# H_D#131
6 H_D#116 I22# D116# H_D#132
6 H_D#117 J22# D117# H_D#133
6 H_D#118 K22# D118# H_D#134
6 H_D#119 L22# D119# H_D#135
6 H_D#120 M22# D120# H_D#136
6 H_D#121 N22# D121# H_D#137
6 H_D#122 O22# D122# H_D#138
6 H_D#123 P22# D123# H_D#139
6 H_D#124 Q22# D124# H_D#140
6 H_D#125 R22# D125# H_D#141
6 H_D#126 S22# D126# H_D#142
6 H_D#127 T22# D127# H_D#143

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#6 <<>> H_DSTBN#6 6
6 H_DSTBP#6 <<>> H_DSTBP#6 6
6 H_DINV#6 <<>> H_DINV#6 6

6 H_D#128 E22# D128# H_D#144
6 H_D#129 F22# D129# H_D#145
6 H_D#130 G22# D130# H_D#146
6 H_D#131 H22# D131# H_D#147
6 H_D#132 I22# D132# H_D#148
6 H_D#133 J22# D133# H_D#149
6 H_D#134 K22# D134# H_D#150
6 H_D#135 L22# D135# H_D#151
6 H_D#136 M22# D136# H_D#152
6 H_D#137 N22# D137# H_D#153
6 H_D#138 O22# D138# H_D#154
6 H_D#139 P22# D139# H_D#155
6 H_D#140 Q22# D140# H_D#156
6 H_D#141 R22# D141# H_D#157
6 H_D#142 S22# D142# H_D#158
6 H_D#143 T22# D143# H_D#159

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#7 <<>> H_DSTBN#7 6
6 H_DSTBP#7 <<>> H_DSTBP#7 6
6 H_DINV#7 <<>> H_DINV#7 6

6 H_D#144 E22# D144# H_D#160
6 H_D#145 F22# D145# H_D#161
6 H_D#146 G22# D146# H_D#162
6 H_D#147 H22# D147# H_D#163
6 H_D#148 I22# D148# H_D#164
6 H_D#149 J22# D149# H_D#165
6 H_D#150 K22# D150# H_D#166
6 H_D#151 L22# D151# H_D#167
6 H_D#152 M22# D152# H_D#168
6 H_D#153 N22# D153# H_D#169
6 H_D#154 O22# D154# H_D#170
6 H_D#155 P22# D155# H_D#171
6 H_D#156 Q22# D156# H_D#172
6 H_D#157 R22# D157# H_D#173
6 H_D#158 S22# D158# H_D#174
6 H_D#159 T22# D159# H_D#175

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#8 <<>> H_DSTBN#8 6
6 H_DSTBP#8 <<>> H_DSTBP#8 6
6 H_DINV#8 <<>> H_DINV#8 6

6 H_D#160 E22# D160# H_D#176
6 H_D#161 F22# D161# H_D#177
6 H_D#162 G22# D162# H_D#178
6 H_D#163 H22# D163# H_D#179
6 H_D#164 I22# D164# H_D#180
6 H_D#165 J22# D165# H_D#181
6 H_D#166 K22# D166# H_D#182
6 H_D#167 L22# D167# H_D#183
6 H_D#168 M22# D168# H_D#184
6 H_D#169 N22# D169# H_D#185
6 H_D#170 O22# D170# H_D#186
6 H_D#171 P22# D171# H_D#187
6 H_D#172 Q22# D172# H_D#188
6 H_D#173 R22# D173# H_D#189
6 H_D#174 S22# D174# H_D#190
6 H_D#175 T22# D175# H_D#191

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#9 <<>> H_DSTBN#9 6
6 H_DSTBP#9 <<>> H_DSTBP#9 6
6 H_DINV#9 <<>> H_DINV#9 6

6 H_D#176 E22# D176# H_D#192
6 H_D#177 F22# D177# H_D#193
6 H_D#178 G22# D178# H_D#194
6 H_D#179 H22# D179# H_D#195
6 H_D#180 I22# D180# H_D#196
6 H_D#181 J22# D181# H_D#197
6 H_D#182 K22# D182# H_D#198
6 H_D#183 L22# D183# H_D#199
6 H_D#184 M22# D184# H_D#200
6 H_D#185 N22# D185# H_D#201
6 H_D#186 O22# D186# H_D#202
6 H_D#187 P22# D187# H_D#203
6 H_D#188 Q22# D188# H_D#204
6 H_D#189 R22# D189# H_D#205
6 H_D#190 S22# D190# H_D#206
6 H_D#191 T22# D191# H_D#207

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#10 <<>> H_DSTBN#10 6
6 H_DSTBP#10 <<>> H_DSTBP#10 6
6 H_DINV#10 <<>> H_DINV#10 6

6 H_D#192 E22# D192# H_D#208
6 H_D#193 F22# D193# H_D#209
6 H_D#194 G22# D194# H_D#210
6 H_D#195 H22# D195# H_D#211
6 H_D#196 I22# D196# H_D#212
6 H_D#197 J22# D197# H_D#213
6 H_D#198 K22# D198# H_D#214
6 H_D#199 L22# D199# H_D#215
6 H_D#200 M22# D200# H_D#216
6 H_D#201 N22# D201# H_D#217
6 H_D#202 O22# D202# H_D#218
6 H_D#203 P22# D203# H_D#219
6 H_D#204 Q22# D204# H_D#220
6 H_D#205 R22# D205# H_D#221
6 H_D#206 S22# D206# H_D#222
6 H_D#207 T22# D207# H_D#223

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#11 <<>> H_DSTBN#11 6
6 H_DSTBP#11 <<>> H_DSTBP#11 6
6 H_DINV#11 <<>> H_DINV#11 6

6 H_D#208 E22# D208# H_D#224
6 H_D#209 F22# D209# H_D#225
6 H_D#210 G22# D210# H_D#226
6 H_D#211 H22# D211# H_D#227
6 H_D#212 I22# D212# H_D#228
6 H_D#213 J22# D213# H_D#229
6 H_D#214 K22# D214# H_D#230
6 H_D#215 L22# D215# H_D#231
6 H_D#216 M22# D216# H_D#232
6 H_D#217 N22# D217# H_D#233
6 H_D#218 O22# D218# H_D#234
6 H_D#219 P22# D219# H_D#235
6 H_D#220 Q22# D220# H_D#236
6 H_D#221 R22# D221# H_D#237
6 H_D#222 S22# D222# H_D#238
6 H_D#223 T22# D223# H_D#239

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#12 <<>> H_DSTBN#12 6
6 H_DSTBP#12 <<>> H_DSTBP#12 6
6 H_DINV#12 <<>> H_DINV#12 6

6 H_D#224 E22# D224# H_D#240
6 H_D#225 F22# D225# H_D#241
6 H_D#226 G22# D226# H_D#242
6 H_D#227 H22# D227# H_D#243
6 H_D#228 I22# D228# H_D#244
6 H_D#229 J22# D229# H_D#245
6 H_D#230 K22# D230# H_D#246
6 H_D#231 L22# D231# H_D#247
6 H_D#232 M22# D232# H_D#248
6 H_D#233 N22# D233# H_D#249
6 H_D#234 O22# D234# H_D#250
6 H_D#235 P22# D235# H_D#251
6 H_D#236 Q22# D236# H_D#252
6 H_D#237 R22# D237# H_D#253
6 H_D#238 S22# D238# H_D#254
6 H_D#239 T22# D239# H_D#255

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#13 <<>> H_DSTBN#13 6
6 H_DSTBP#13 <<>> H_DSTBP#13 6
6 H_DINV#13 <<>> H_DINV#13 6

6 H_D#240 E22# D240# H_D#256
6 H_D#241 F22# D241# H_D#257
6 H_D#242 G22# D242# H_D#258
6 H_D#243 H22# D243# H_D#259
6 H_D#244 I22# D244# H_D#260
6 H_D#245 J22# D245# H_D#261
6 H_D#246 K22# D246# H_D#262
6 H_D#247 L22# D247# H_D#263
6 H_D#248 M22# D248# H_D#264
6 H_D#249 N22# D249# H_D#265
6 H_D#250 O22# D250# H_D#266
6 H_D#251 P22# D251# H_D#267
6 H_D#252 Q22# D252# H_D#268
6 H_D#253 R22# D253# H_D#269
6 H_D#254 S22# D254# H_D#270
6 H_D#255 T22# D255# H_D#271

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#14 <<>> H_DSTBN#14 6
6 H_DSTBP#14 <<>> H_DSTBP#14 6
6 H_DINV#14 <<>> H_DINV#14 6

6 H_D#256 E22# D256# H_D#272
6 H_D#257 F22# D257# H_D#273
6 H_D#258 G22# D258# H_D#274
6 H_D#259 H22# D259# H_D#275
6 H_D#260 I22# D260# H_D#276
6 H_D#261 J22# D261# H_D#277
6 H_D#262 K22# D262# H_D#278
6 H_D#263 L22# D263# H_D#279
6 H_D#264 M22# D264# H_D#280
6 H_D#265 N22# D265# H_D#281
6 H_D#266 O22# D266# H_D#282
6 H_D#267 P22# D267# H_D#283
6 H_D#268 Q22# D268# H_D#284
6 H_D#269 R22# D269# H_D#285
6 H_D#270 S22# D270# H_D#286
6 H_D#271 T22# D271# H_D#287

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#15 <<>> H_DSTBN#15 6
6 H_DSTBP#15 <<>> H_DSTBP#15 6
6 H_DINV#15 <<>> H_DINV#15 6

6 H_D#272 E22# D272# H_D#288
6 H_D#273 F22# D273# H_D#289
6 H_D#274 G22# D274# H_D#290
6 H_D#275 H22# D275# H_D#291
6 H_D#276 I22# D276# H_D#292
6 H_D#277 J22# D277# H_D#293
6 H_D#278 K22# D278# H_D#294
6 H_D#279 L22# D279# H_D#295
6 H_D#280 M22# D280# H_D#296
6 H_D#281 N22# D281# H_D#297
6 H_D#282 O22# D282# H_D#298
6 H_D#283 P22# D283# H_D#299
6 H_D#284 Q22# D284# H_D#300
6 H_D#285 R22# D285# H_D#301
6 H_D#286 S22# D286# H_D#302
6 H_D#287 T22# D287# H_D#303

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#16 <<>> H_DSTBN#16 6
6 H_DSTBP#16 <<>> H_DSTBP#16 6
6 H_DINV#16 <<>> H_DINV#16 6

6 H_D#288 E22# D288# H_D#304
6 H_D#289 F22# D289# H_D#305
6 H_D#290 G22# D290# H_D#306
6 H_D#291 H22# D291# H_D#307
6 H_D#292 I22# D292# H_D#308
6 H_D#293 J22# D293# H_D#309
6 H_D#294 K22# D294# H_D#310
6 H_D#295 L22# D295# H_D#311
6 H_D#296 M22# D296# H_D#312
6 H_D#297 N22# D297# H_D#313
6 H_D#298 O22# D298# H_D#314
6 H_D#299 P22# D299# H_D#315
6 H_D#300 Q22# D300# H_D#316
6 H_D#301 R22# D301# H_D#317
6 H_D#302 S22# D302# H_D#318
6 H_D#303 T22# D303# H_D#319

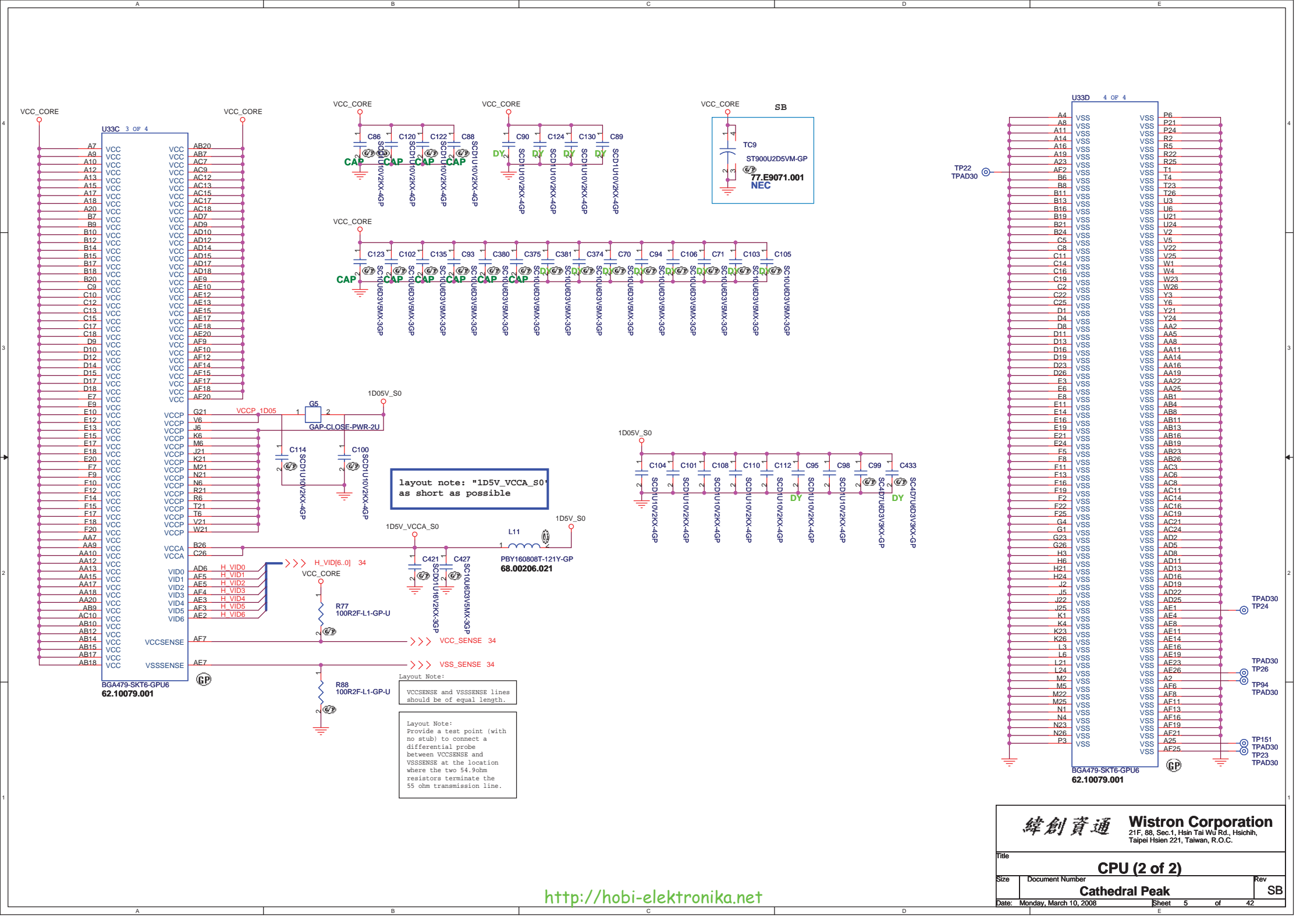
3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

6 H_DSTBN#17 <<>> H_DSTBN#17 6
6 H_DSTBP#17 <<>> H_DSTBP#17 6
6 H_DINV#17 <<>> H_DINV#17 6

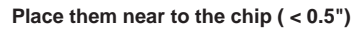
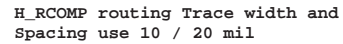
6 H_D#304 E22# D304# H_D#320
6 H_D#305 F22# D305# H_D#321
6 H_D#306 G22# D306# H_D#322
6 H_D#307 H22# D307# H_D#323
6 H_D#308 I22# D308# H_D#324
6 H_D#309 J22# D309# H_D#325
6 H_D#310 K22# D310# H_D#326
6 H_D#311 L22# D311# H_D#327
6 H_D#312 M22# D312# H_D#328
6 H_D#313 N22# D313# H_D#329
6 H_D#314 O22# D314# H_D#330
6 H_D#315 P22# D315# H_D#331
6 H_D#316 Q22# D316# H_D#332
6 H_D#317 R22# D317# H_D#333
6 H_D#318 S22# D318# H_D#334
6 H_D#319 T22# D319# H_D#335

3.7 CPU_SEL0 <<>> B22
3.7 CPU_SEL1 <<>> B23
3.7 CPU_SEL2 <<>> C21

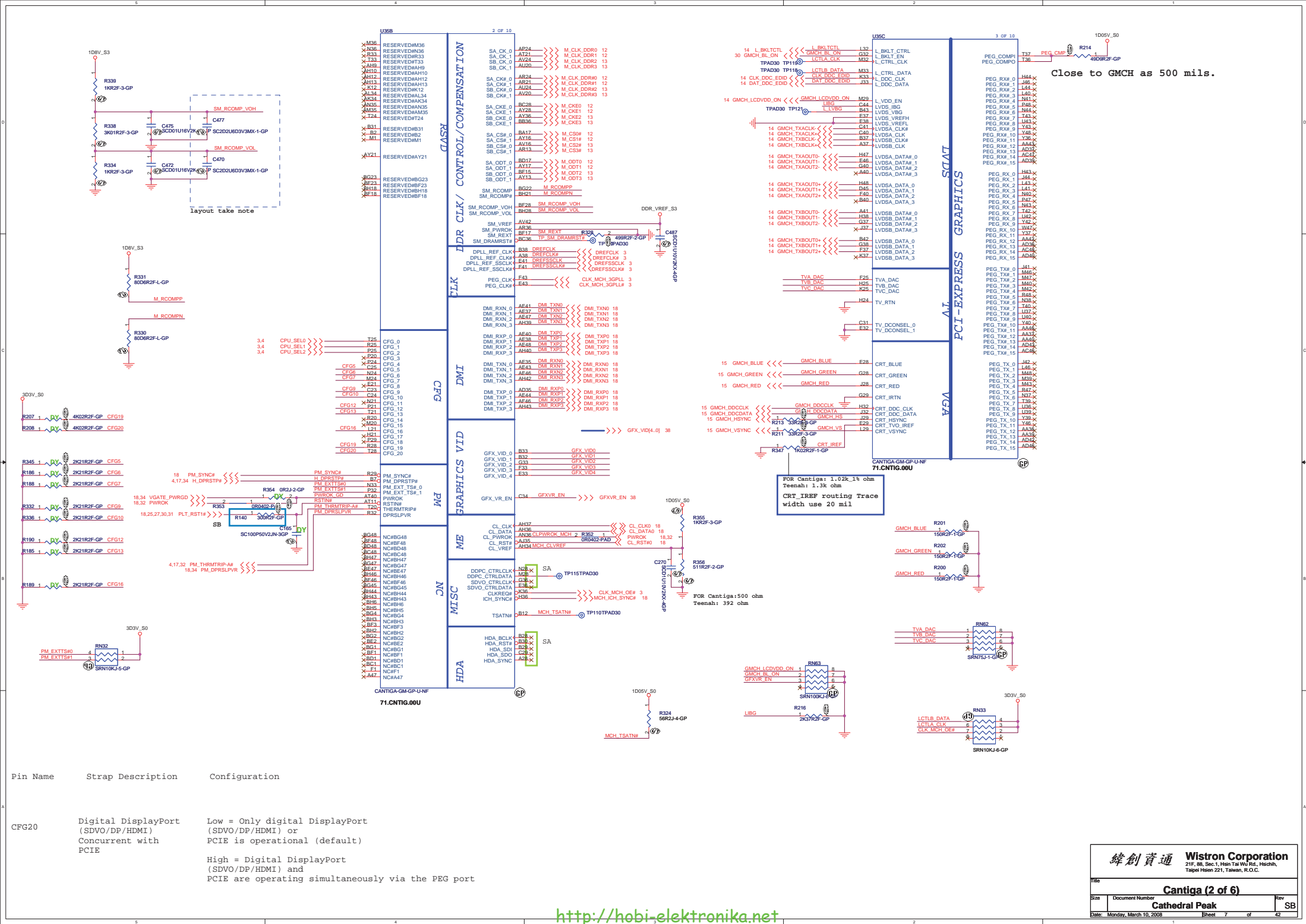
6 H_DSTBN#18 <<>> H_DSTBN#18 6
6 H_DSTBP#18 <<>> H_DSTBP#18 6

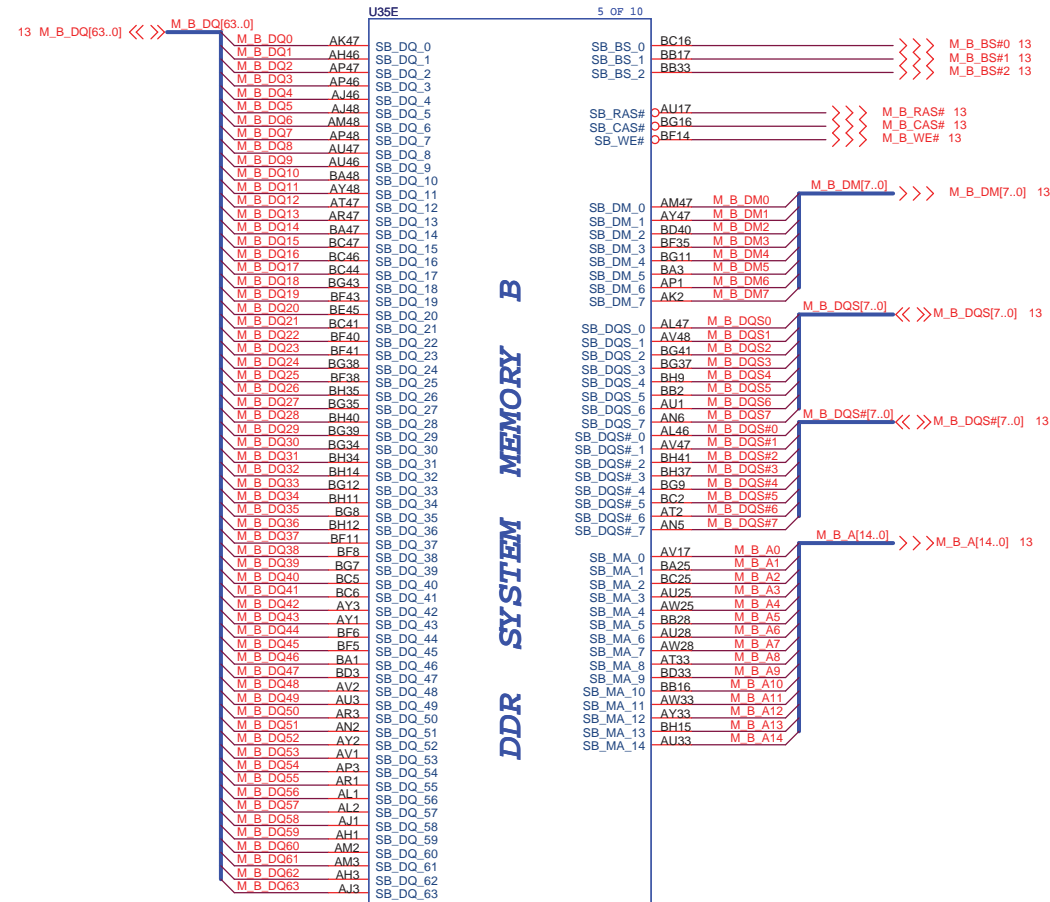
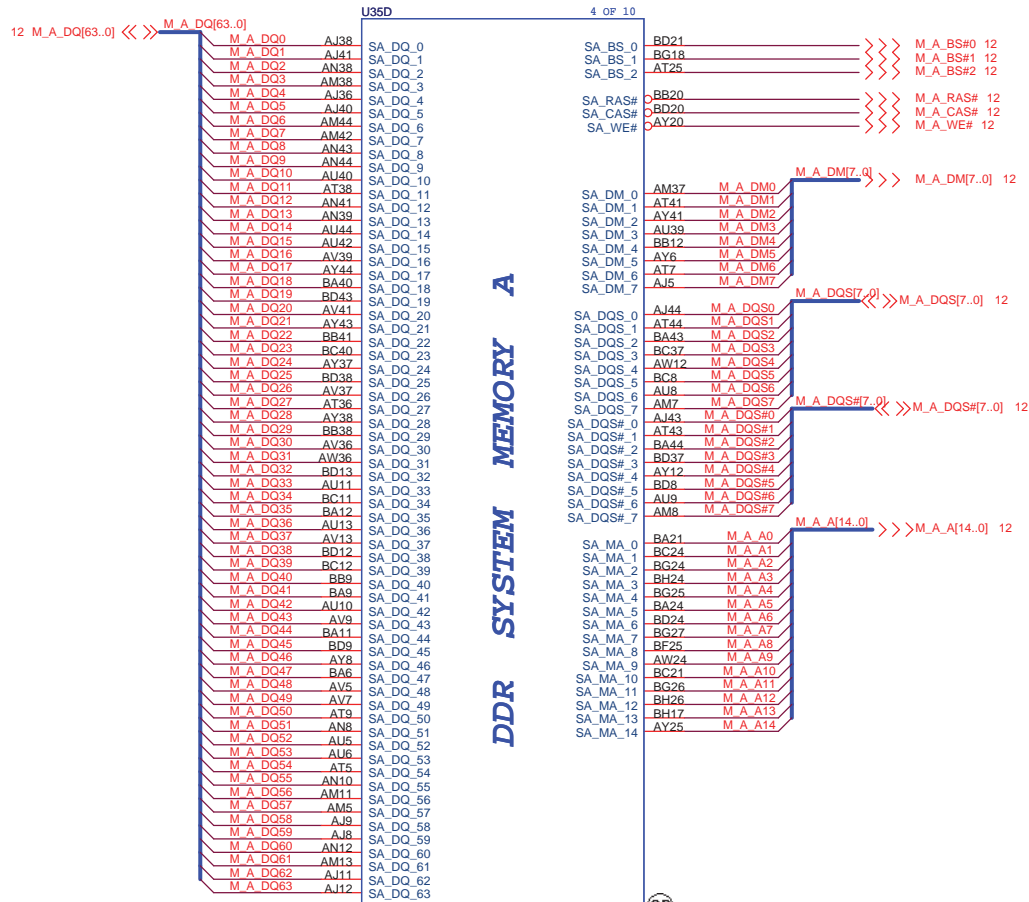


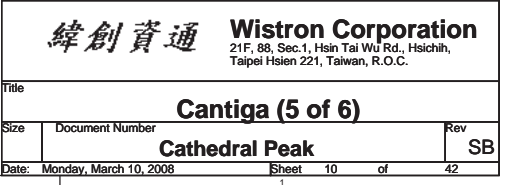
H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)

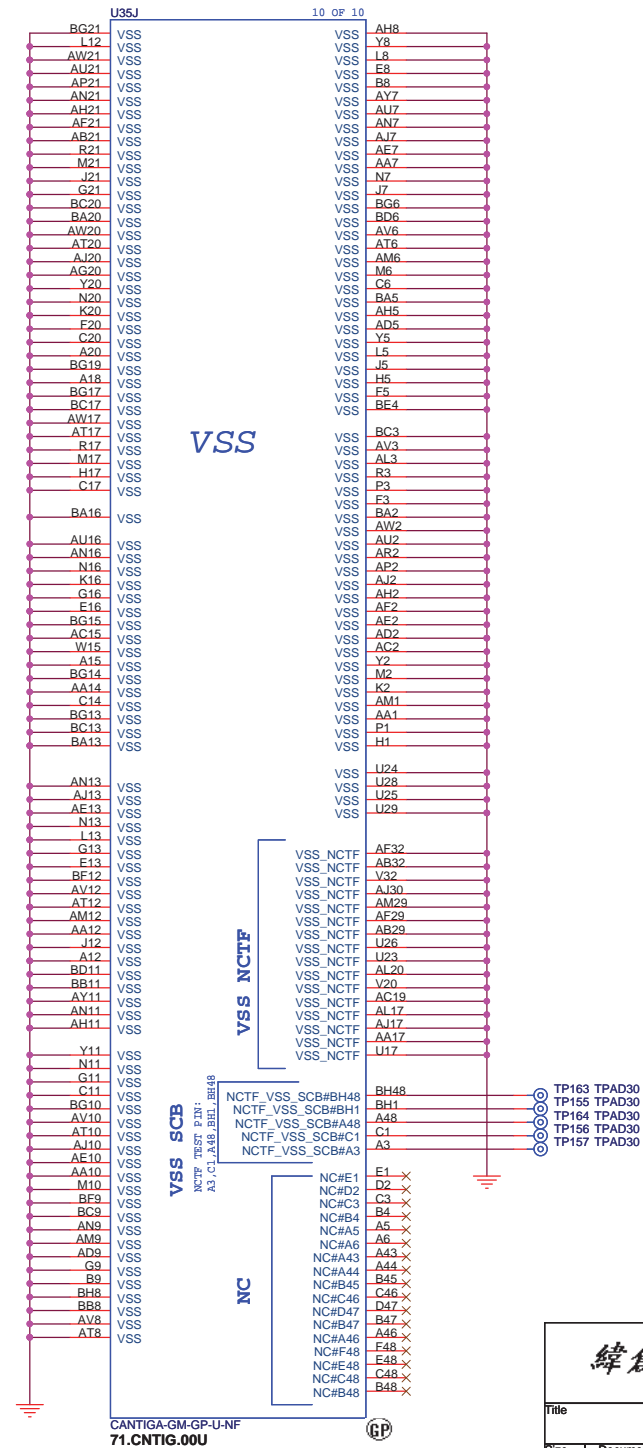
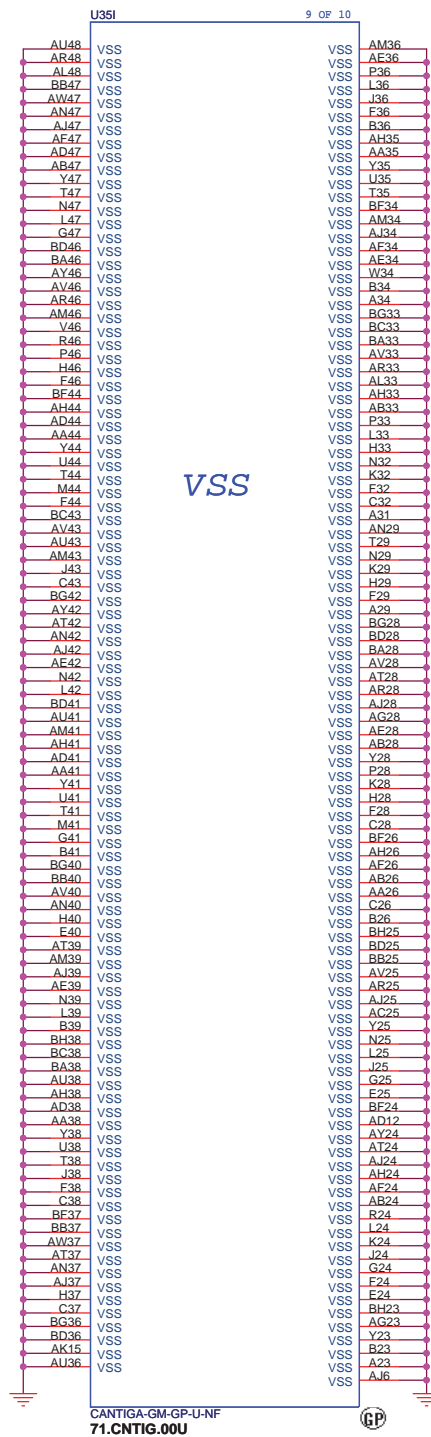


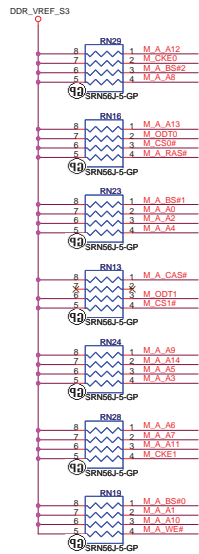
Title			
Cantiga (1 of 6)			
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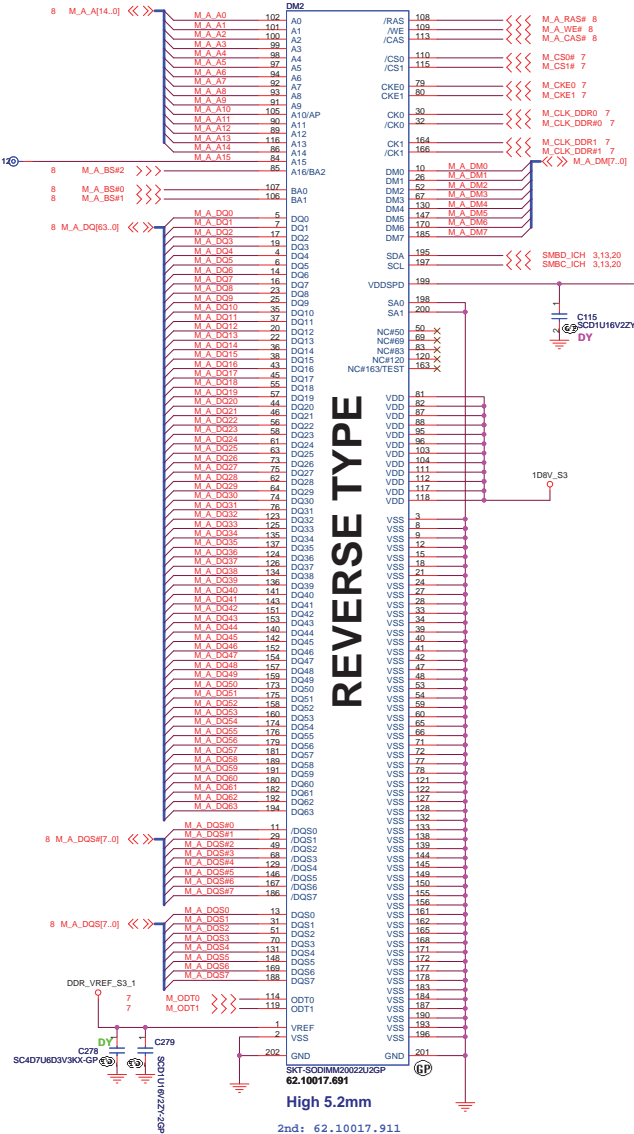
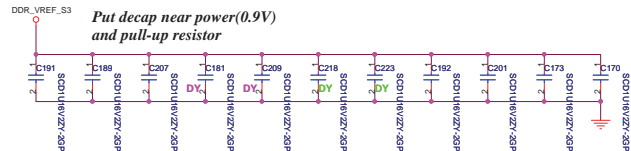


PARALLEL TERMINATION

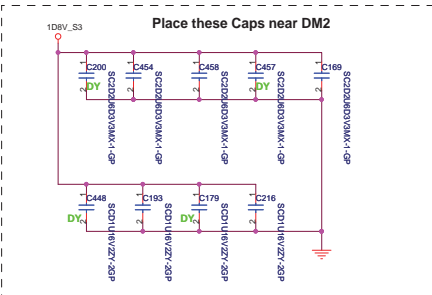
Put decap near power(0.9V) and pull-up resistor

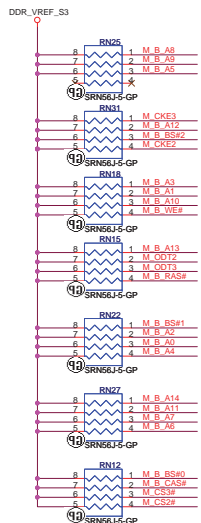
Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



REVERSE TYPE



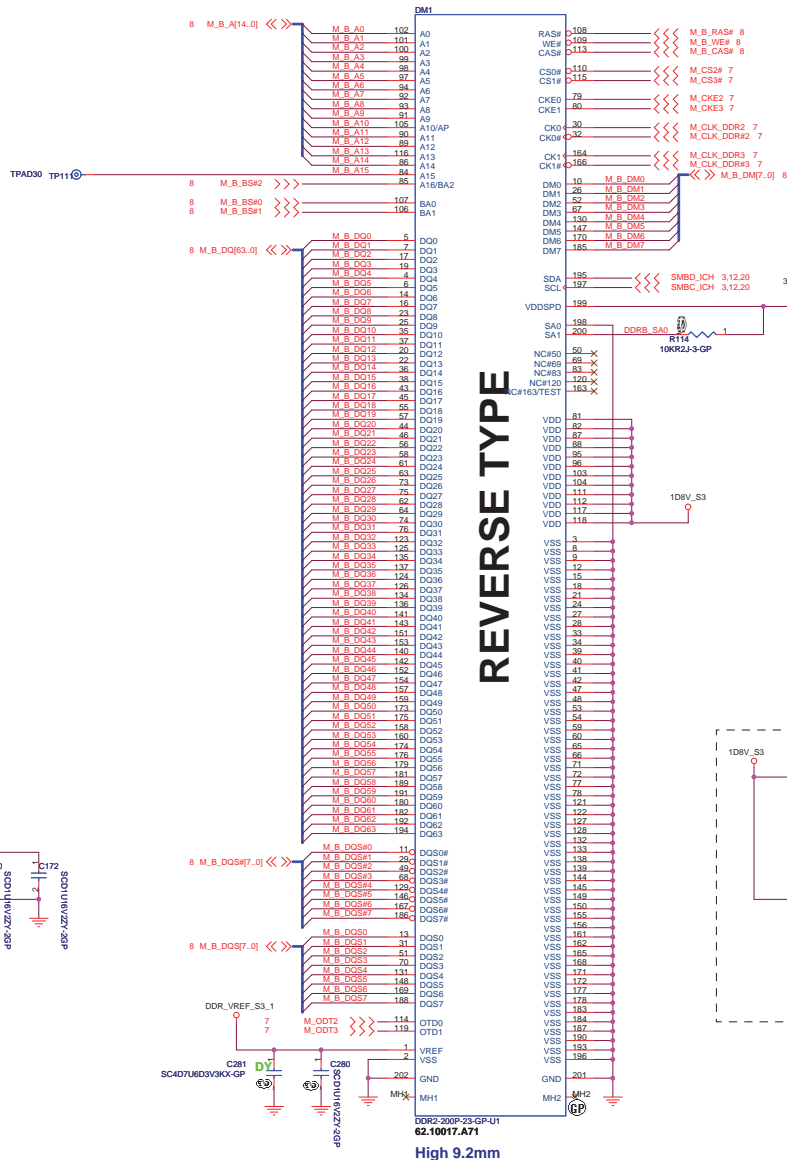
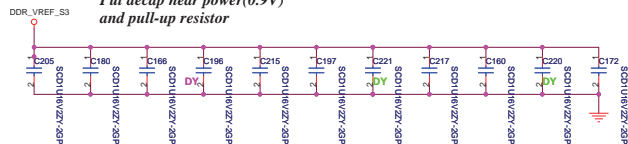


PARALLEL TERMINATION

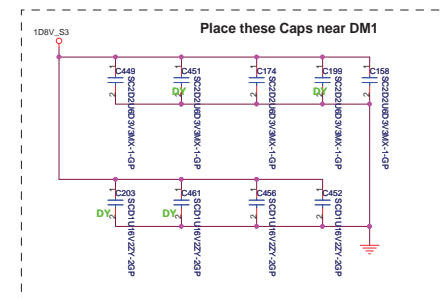
Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



REVERSE TYPE

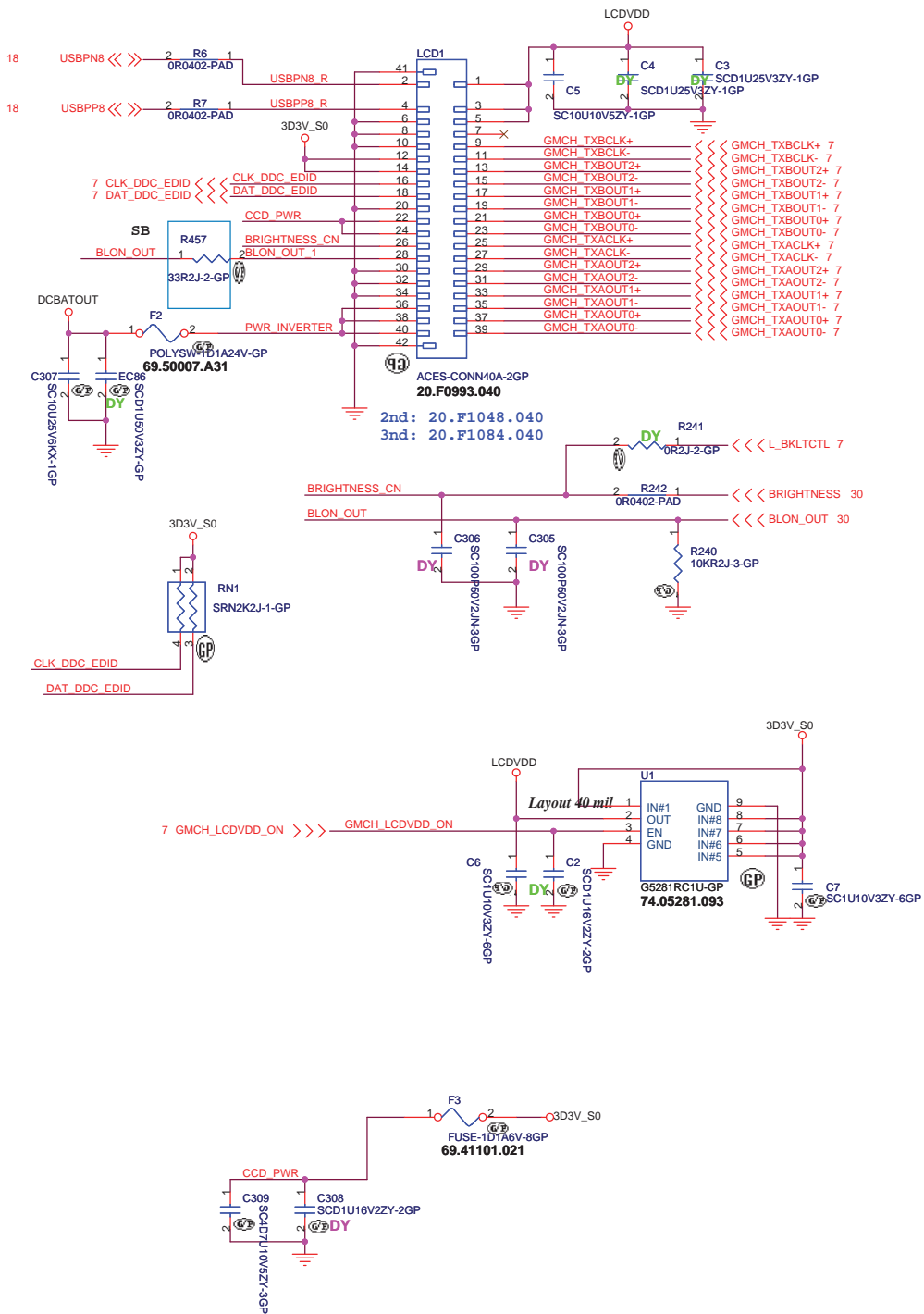


Place these Caps near DM1

High 9.2mm

2nd: 62.10017.B51

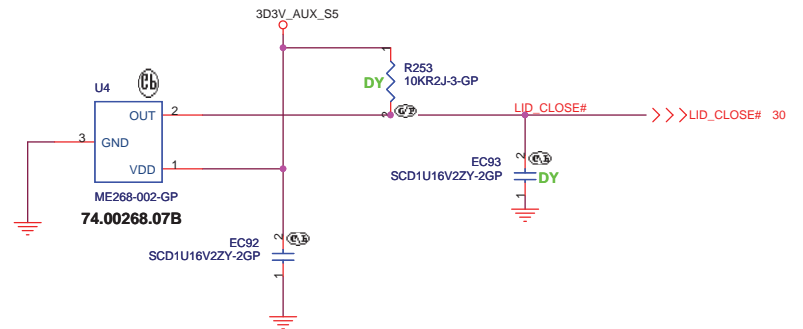
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

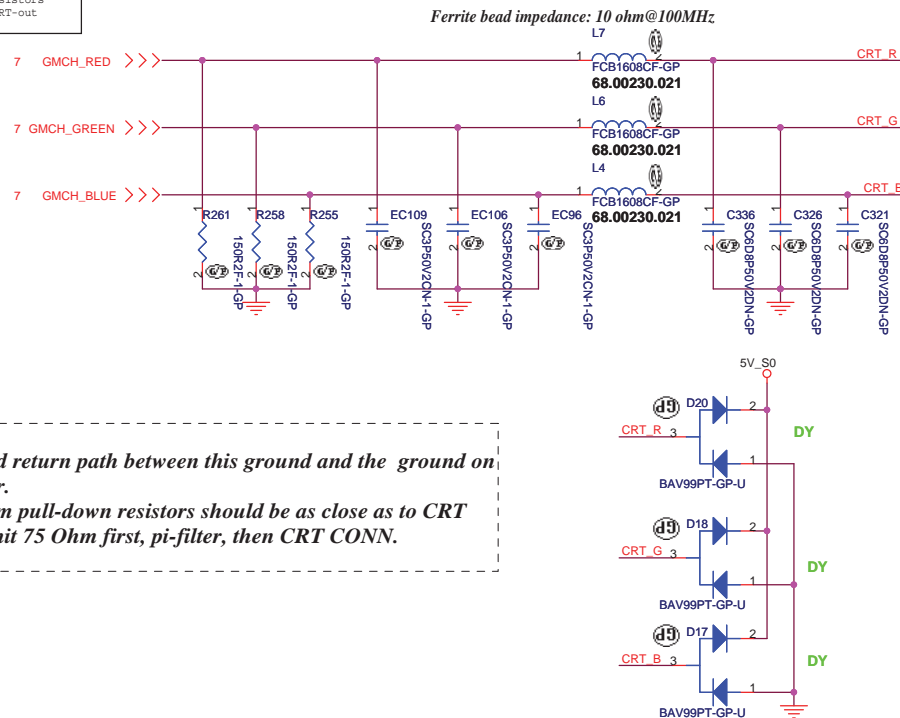
Cover Up Switch



74.00268.A7B

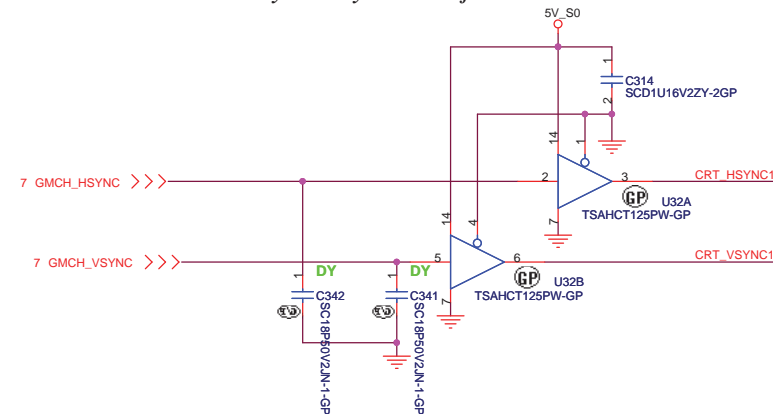
74.00268.C7B

Layout Note:
Place these resistors
close to the CRT-out
connector

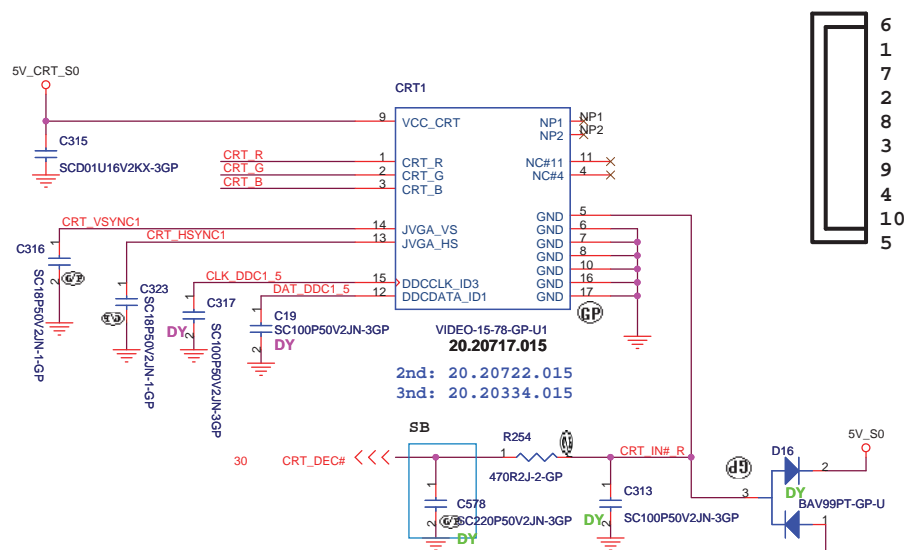


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

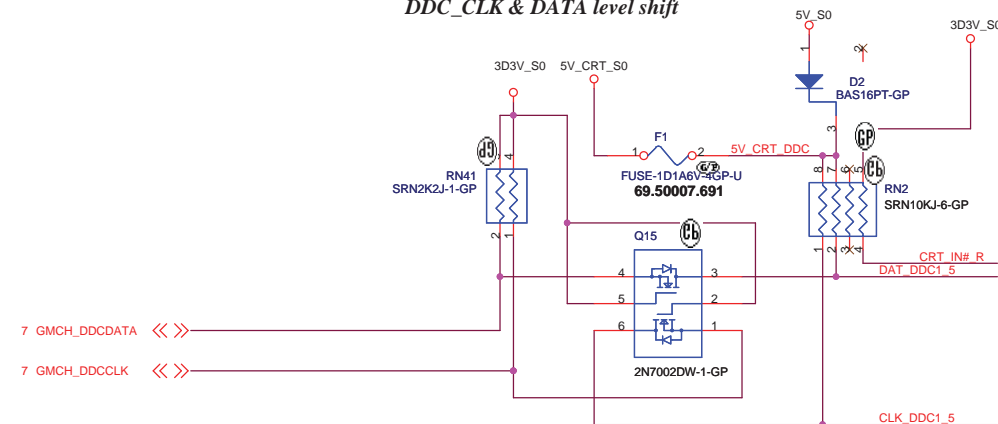
Hsync & Vsync level shift



CRT I/F & CONNECTOR

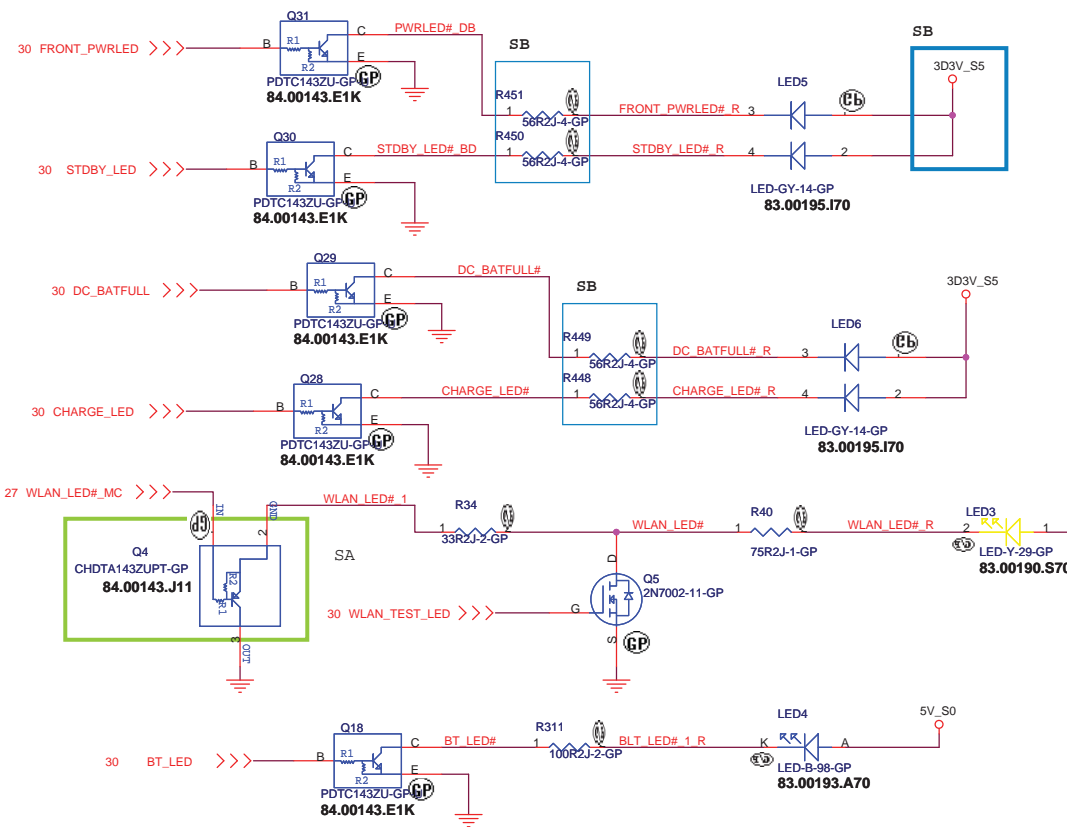


DDC_CLK & DATA level shift

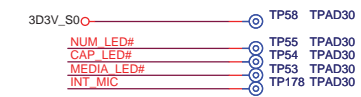
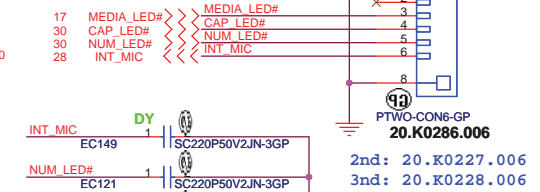
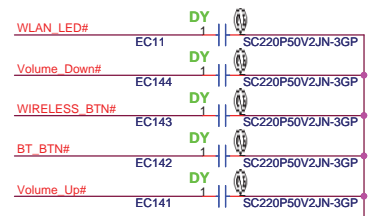
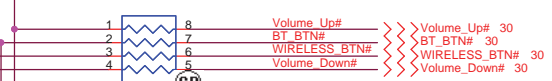
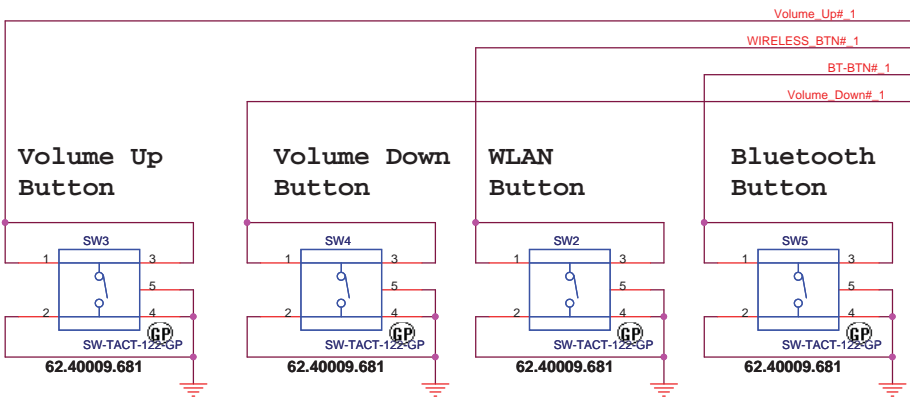
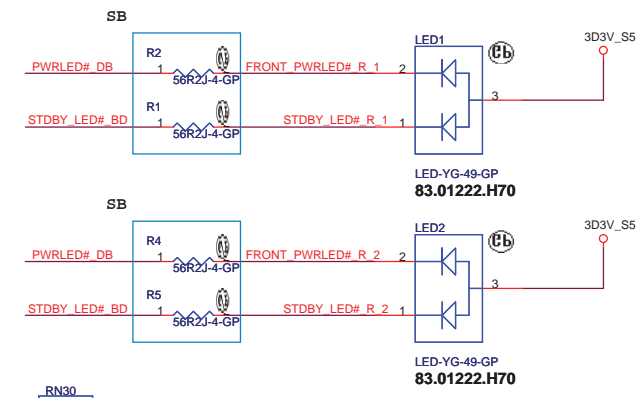
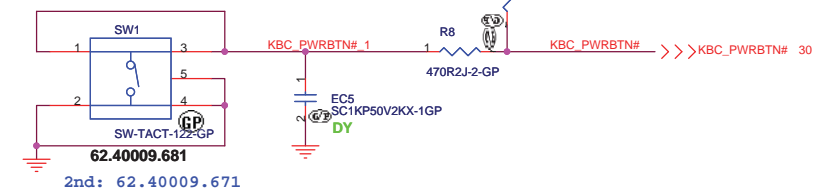


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		CRT Connector	
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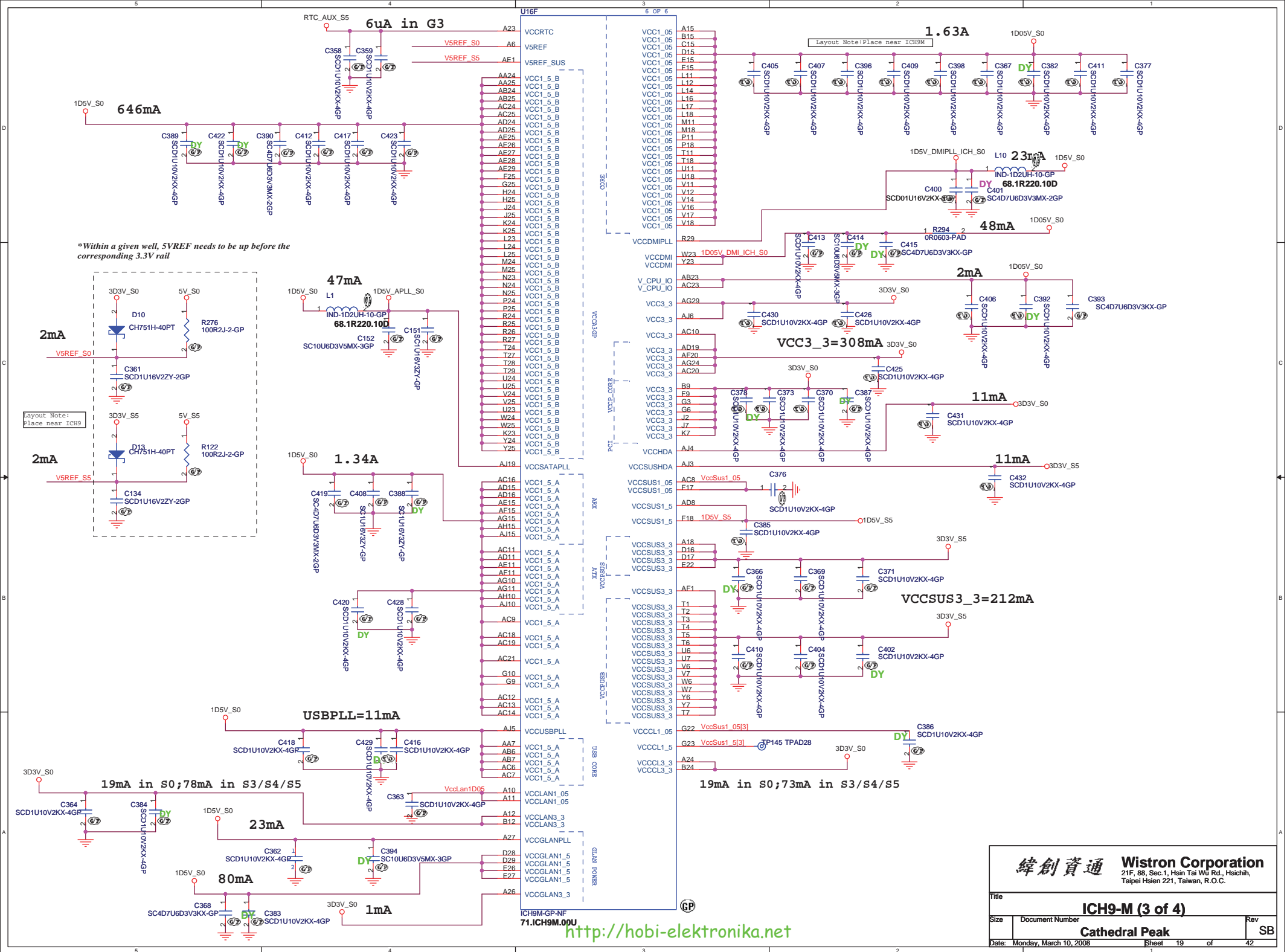
Power Button

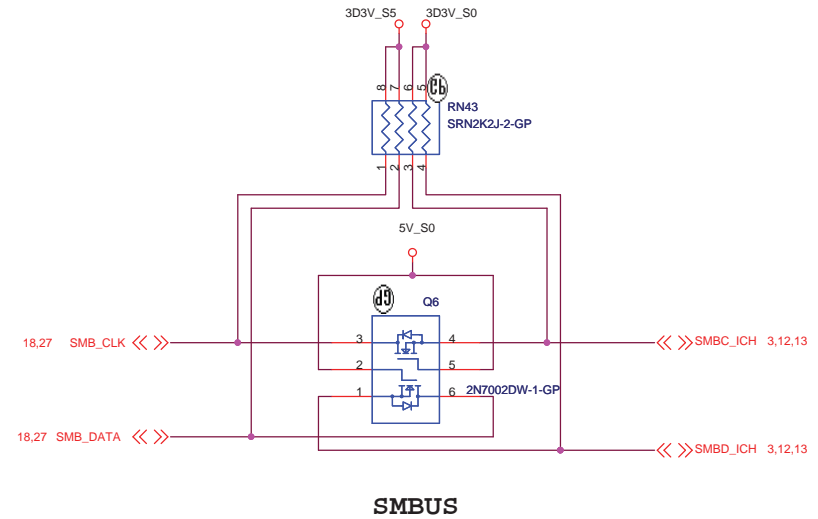
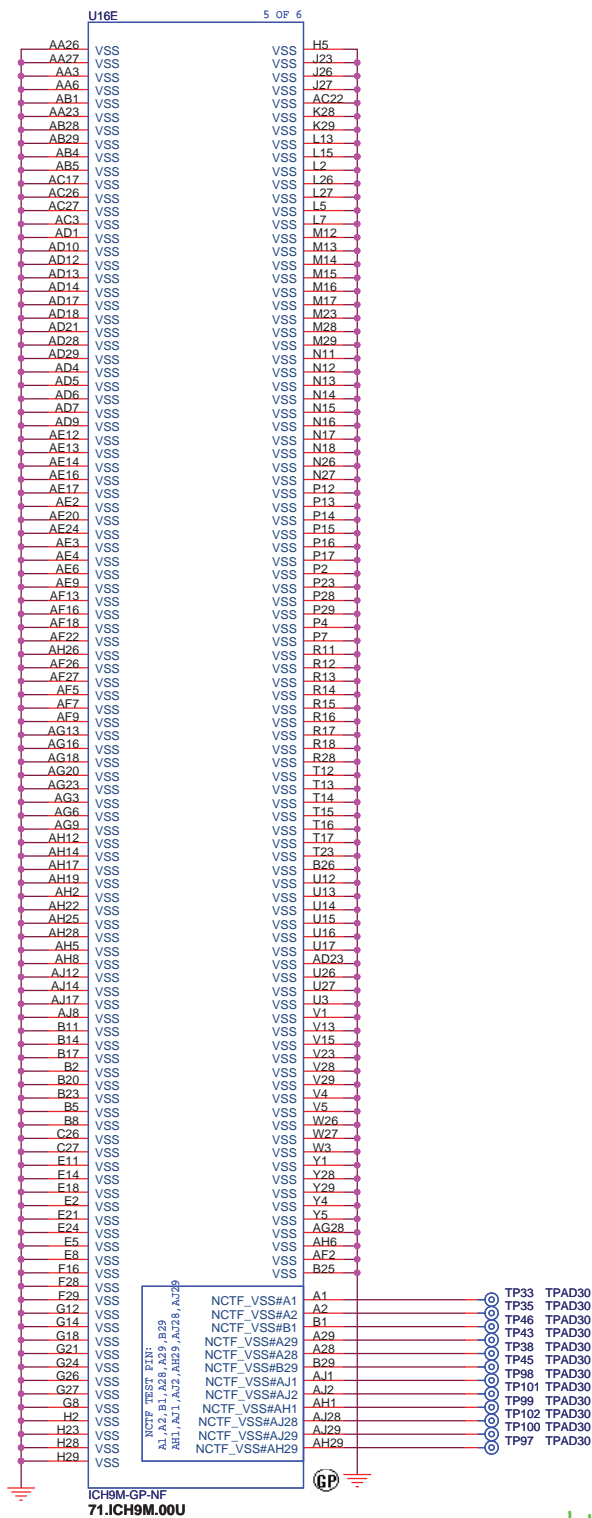


緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

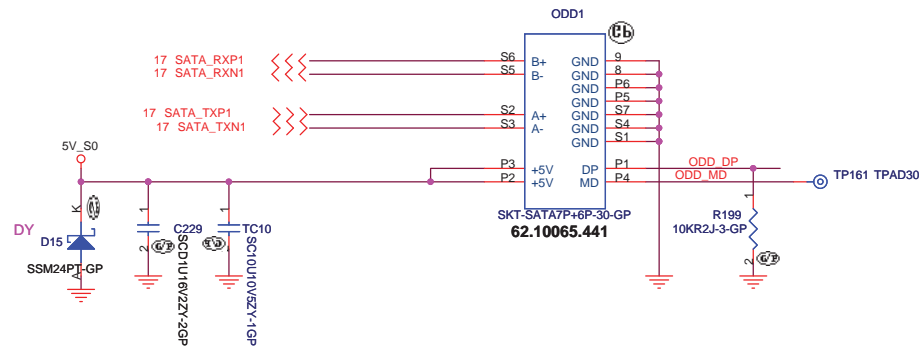
POWER /LAUNCH/LED BOARD			
Size	Document Number	Rev	SB
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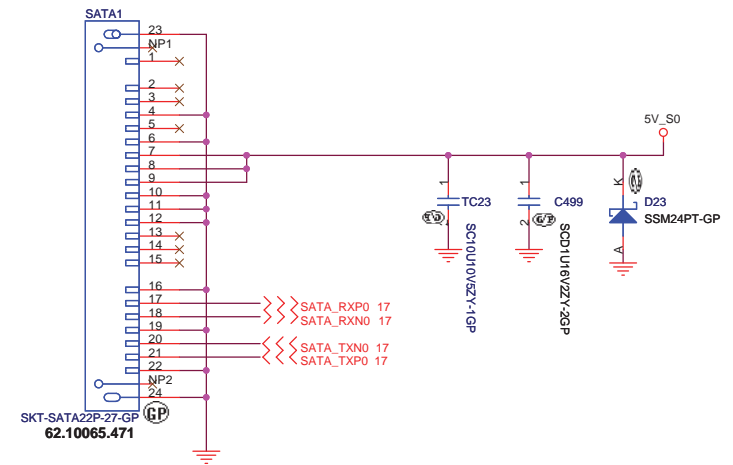




SATA ODD Connector



SATA Connector



Co-Layout Common Mode Choke and 0 Ohm

USB1

USB2

USB3

USB4

USB/BLUETOOTH/MDC

BLUETOOTH MODULE

MDC 1.5 CONN

Wistron Corporation

USB/BLUETOOTH/MDC

Cathedral Peak

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http://hobi-elektronika.net

Co-Layout Common Mode Choke and 0 Ohm

USB1

USB2

USB3

USB4

USB/BLUETOOTH/MDC

BLUETOOTH MODULE

MDC 1.5 CONN

Wistron Corporation

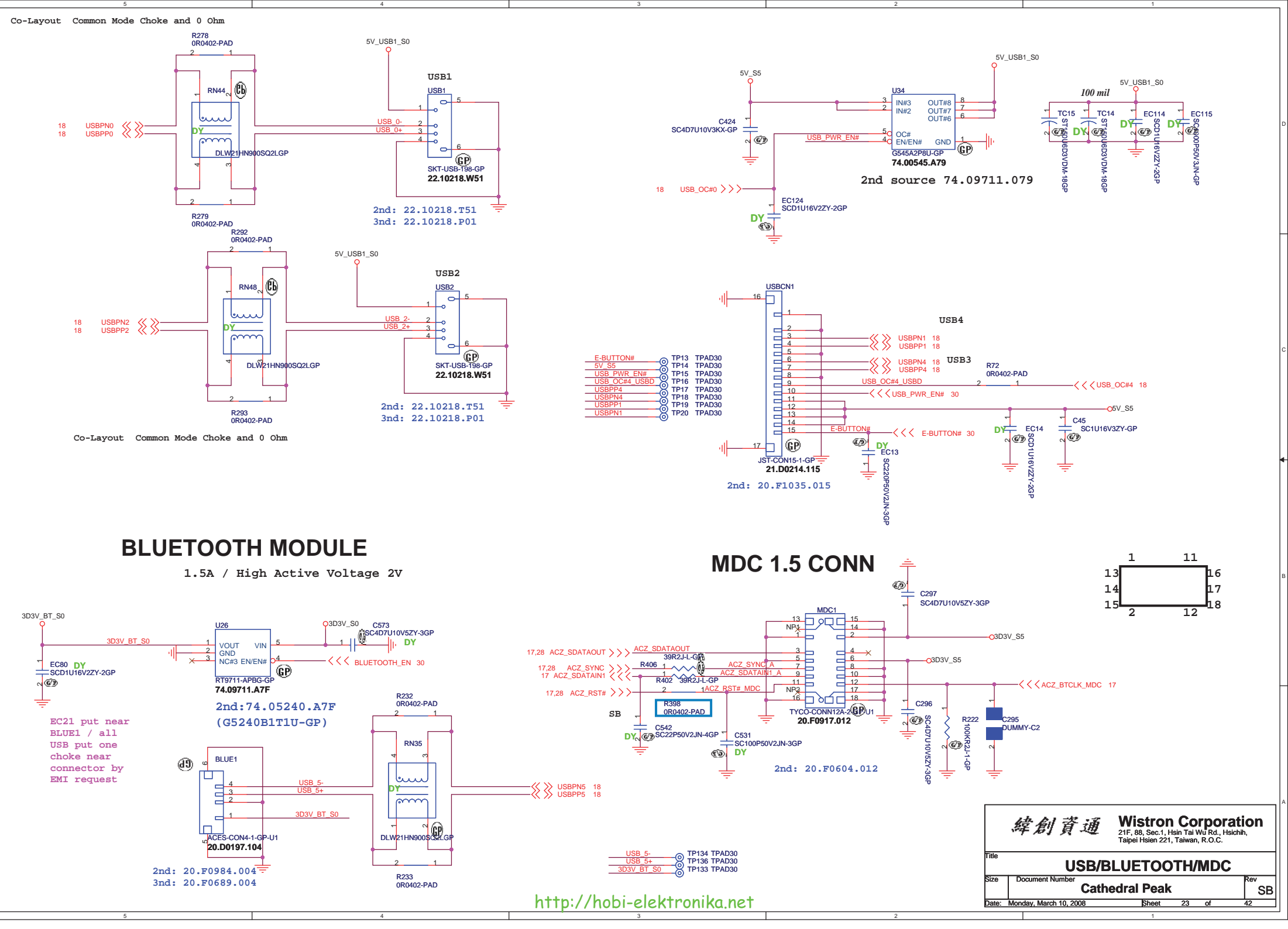
USB/BLUETOOTH/MDC

Cathedral Peak

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http://hobi-elektronika.net



Co-Layout Common Mode Choke and 0 Ohm

USB1

USB2

Co-Layout Common Mode Choke and 0 Ohm

BLUETOOTH MODULE

1.5A / High Active Voltage 2V

MDC 1.5 CONN

USB/BLUETOOTH/MDC

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

USB/BLUETOOTH/MDC

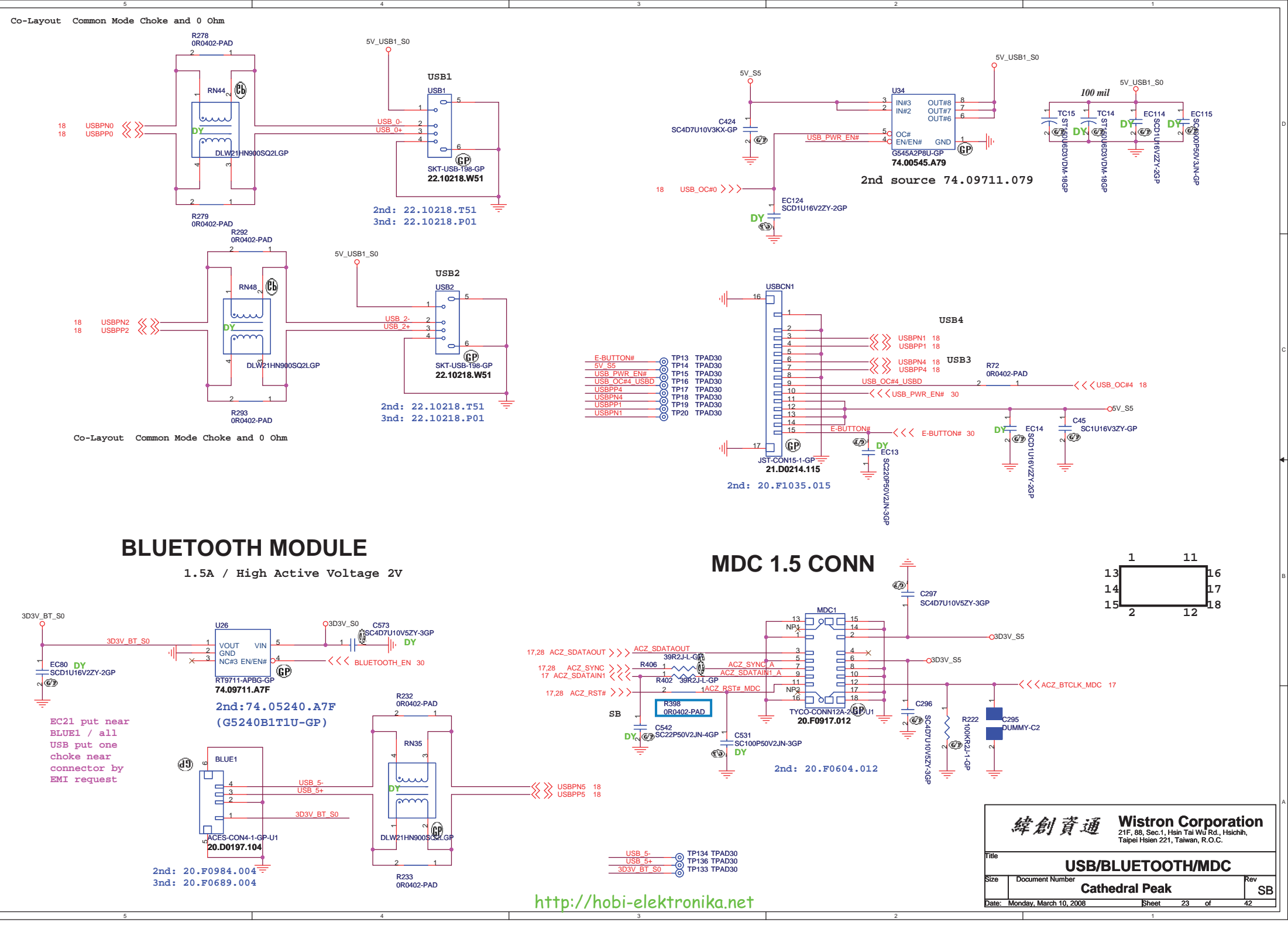
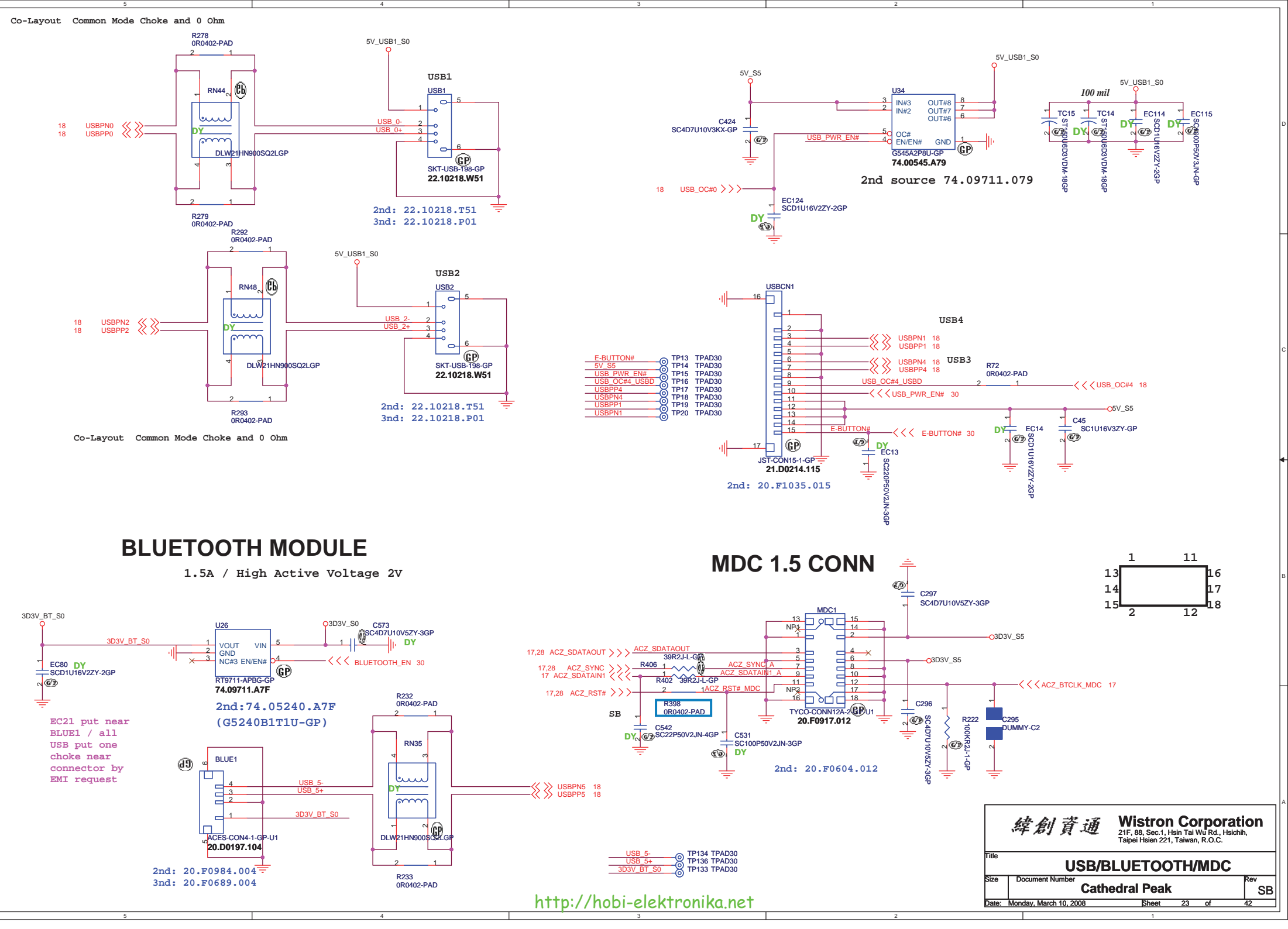
Cathedral Peak

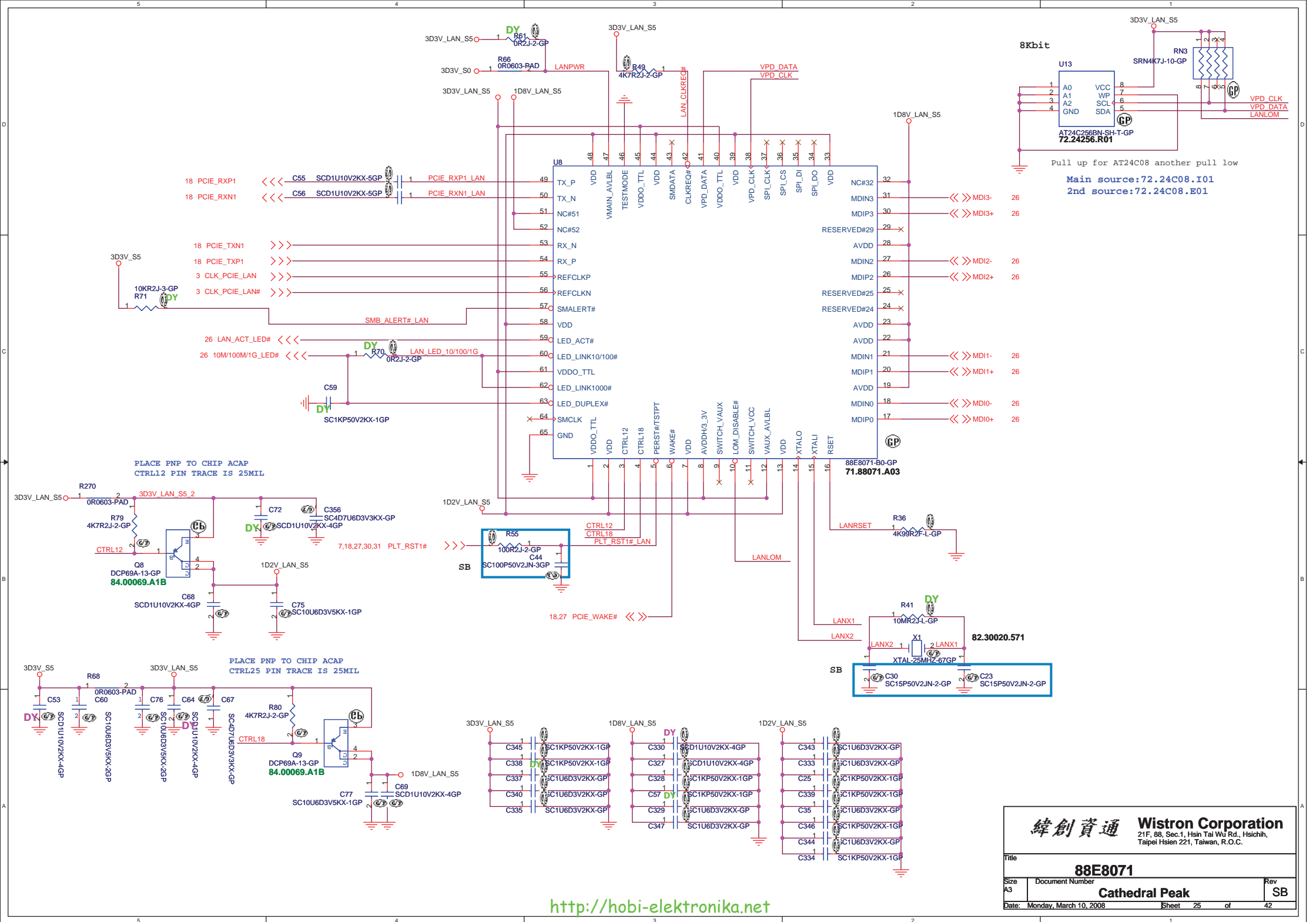
SB

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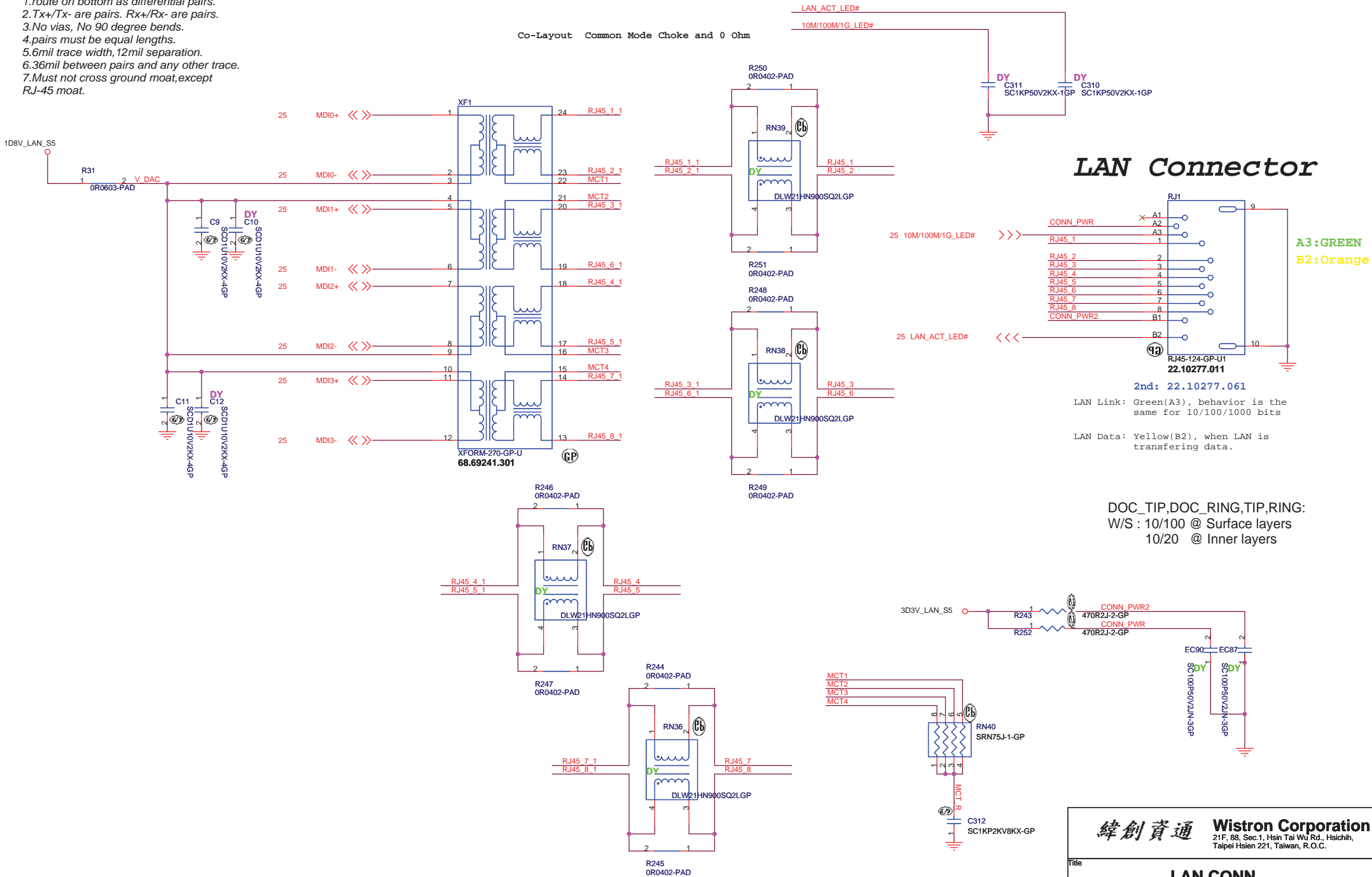




LAN Connector

1. route on bottom as differential pairs.
2. Tx+Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

Co-Layout Common Mode Choke and 0 Ohm

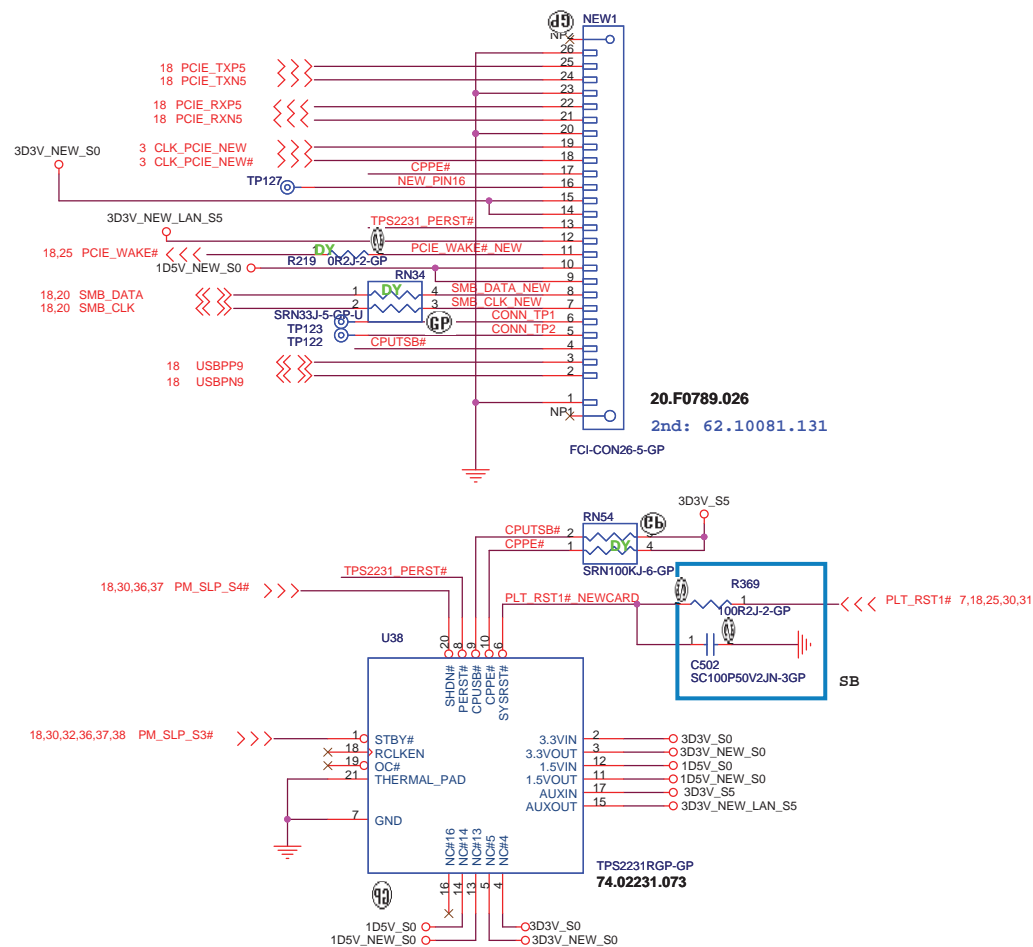


<http://hobi-elektronika.net>

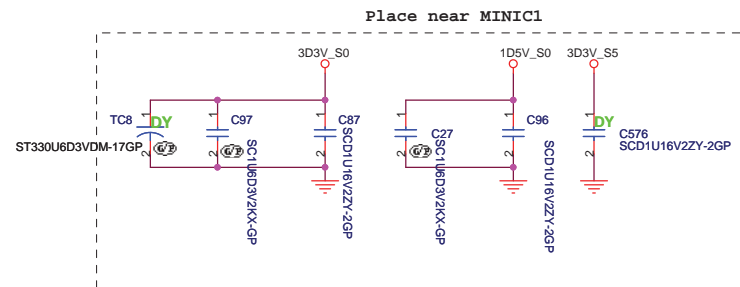
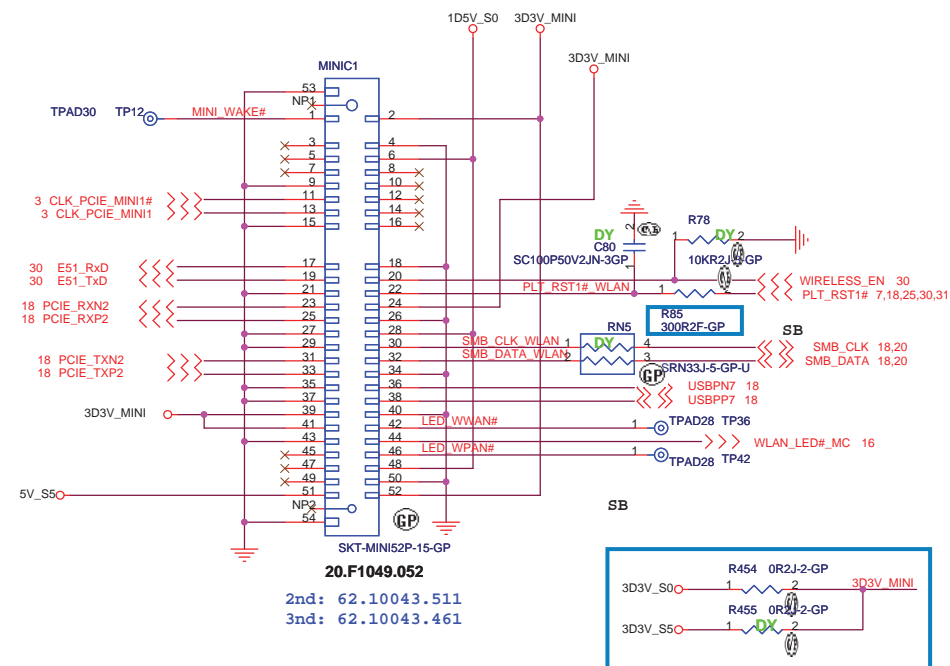
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title			
LAN CONN			
Size A3	Document Number		Rev SE
Cathedral Peak			
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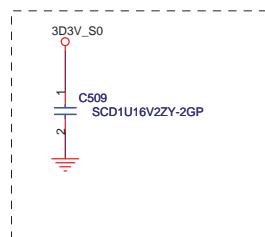
NEWCARD Connector



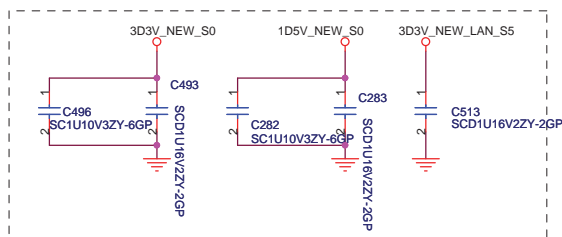
Mini Card Connector(WLAN)



Place them Near to Chip



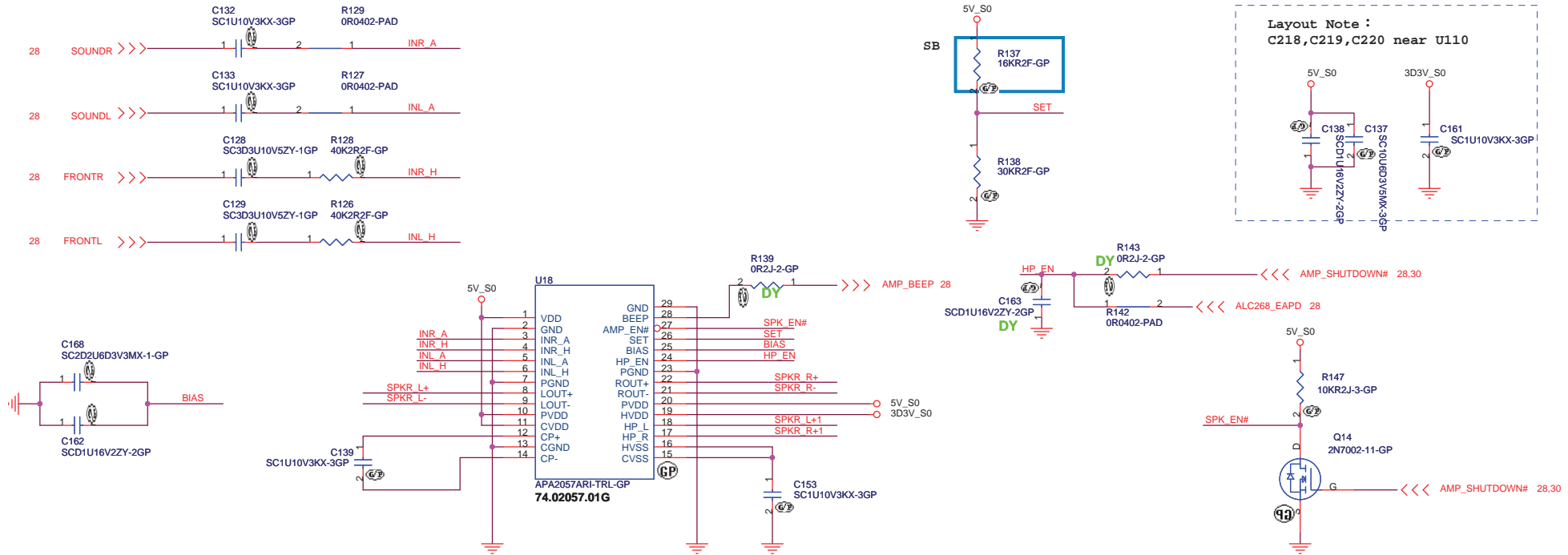
Place them Near to Connector



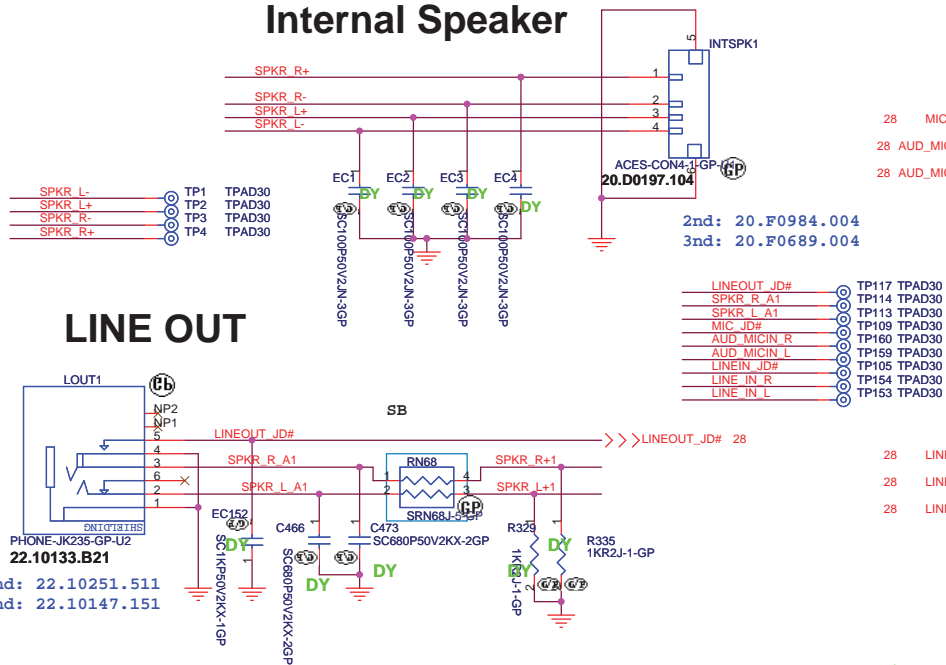
<http://hobi-elektronika.net>

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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NEW CARD/MINI CARD			
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		SB	

AUDIO OP AMPLIFIER

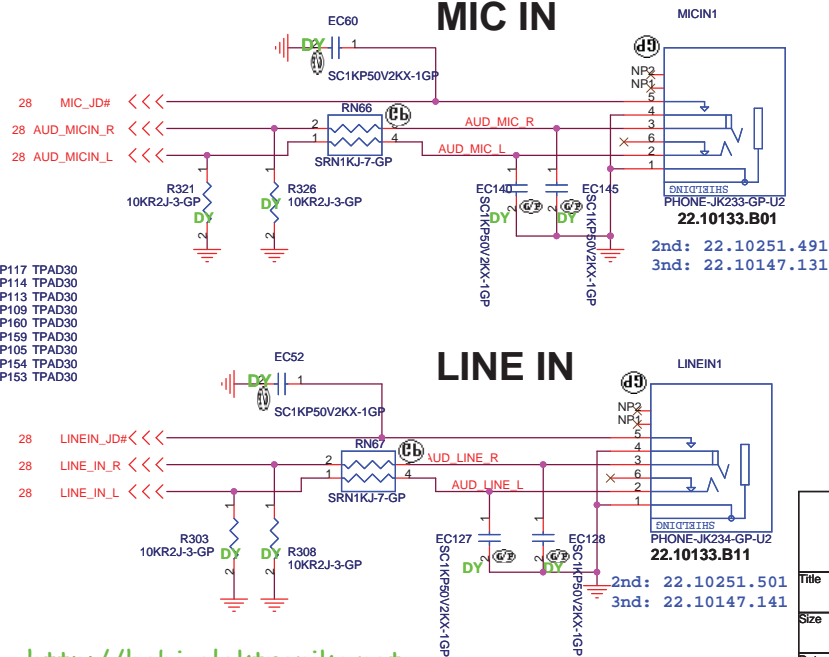


Internal Speaker



LINE OUT

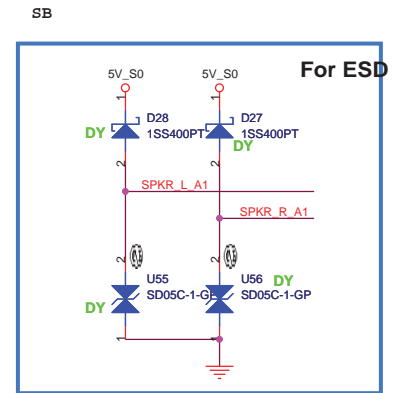
MIC IN



LINE IN

Analog Int. Mic

remove to LED Board

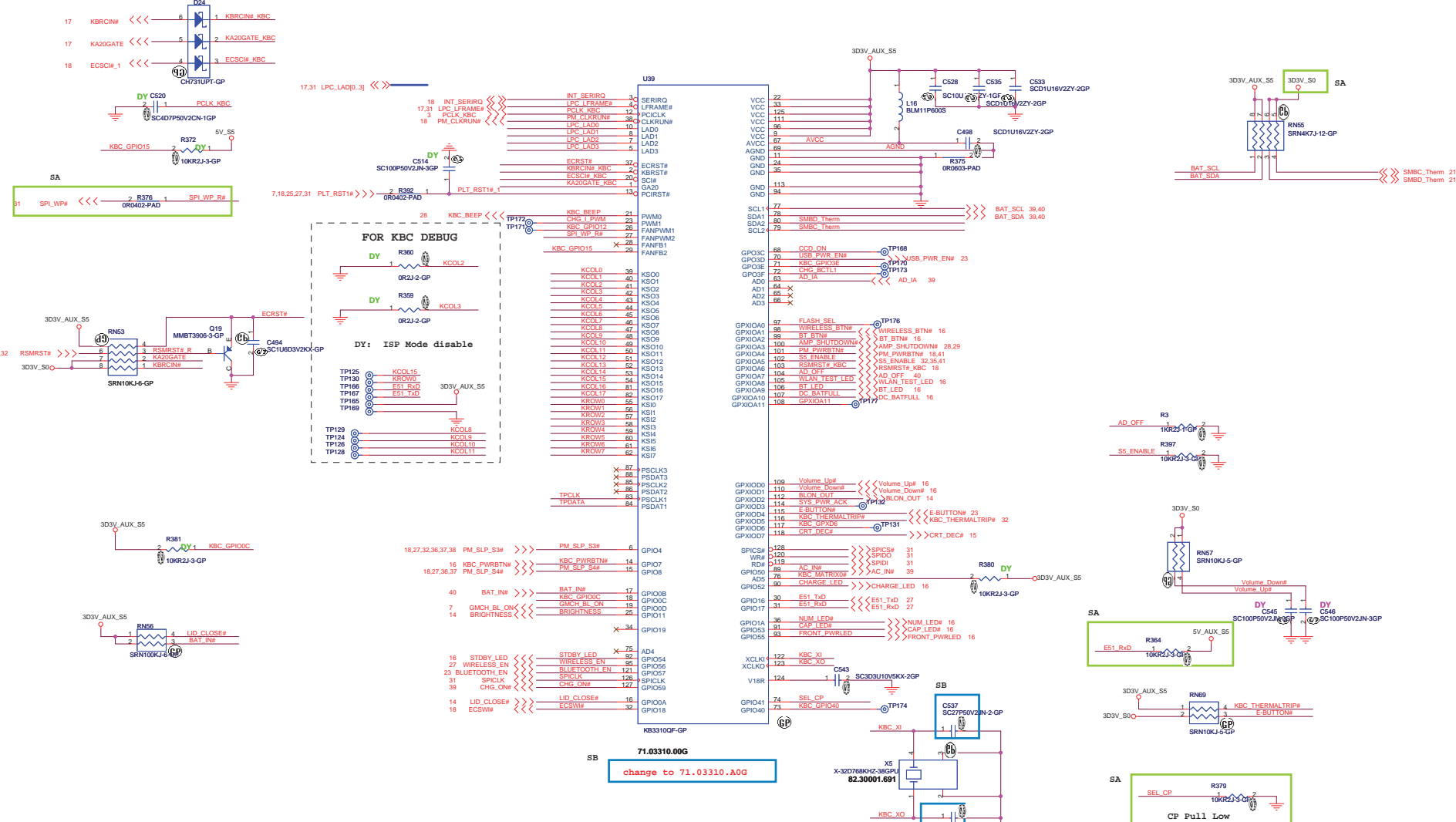


For ESD

緯創資通

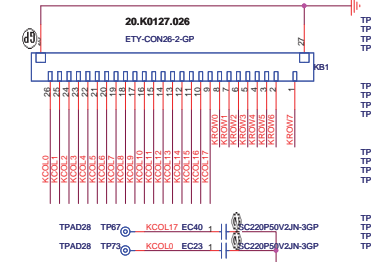
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Title			
AUDIO AMP AND JACK			
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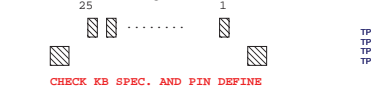


2nd: 20.K0251.026

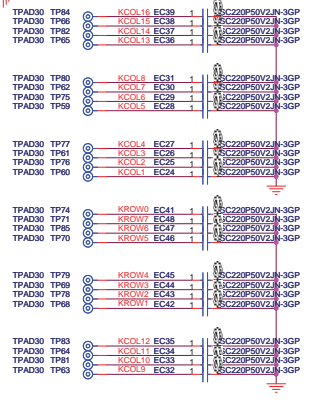
Internal Keyboard Connector



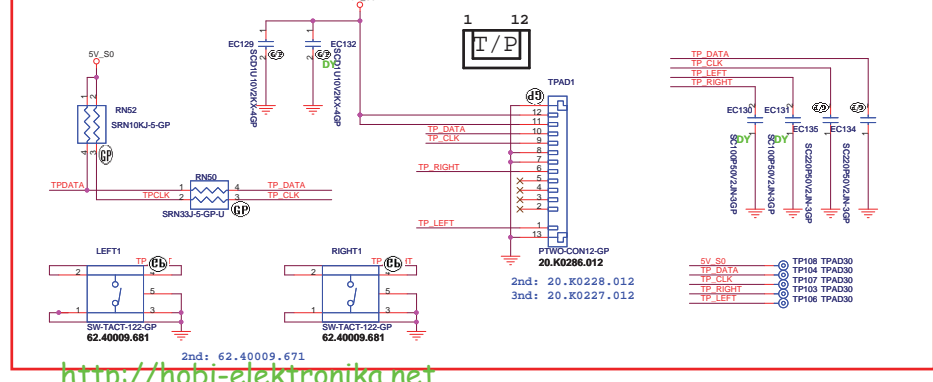
Internal Keyboard CONN

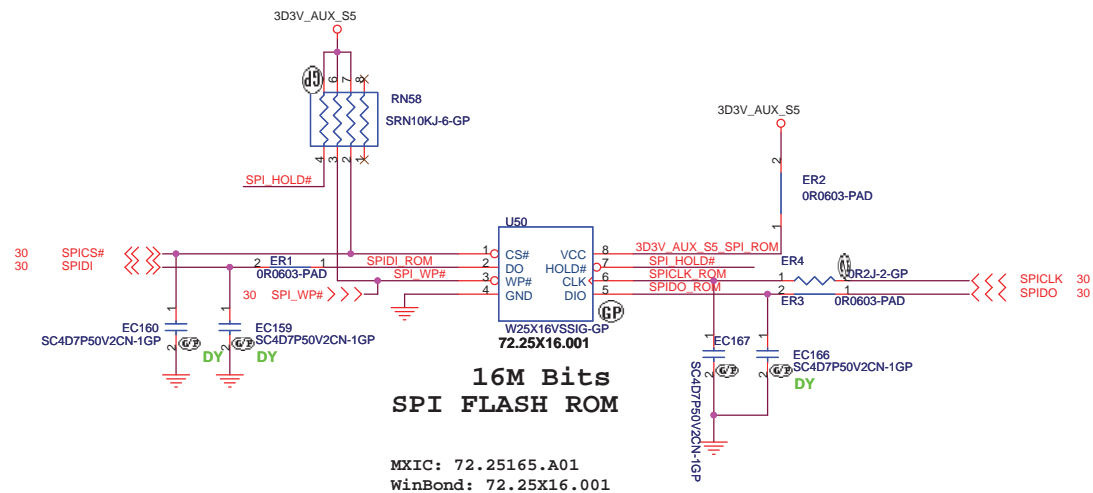


EMI Bypass cap.

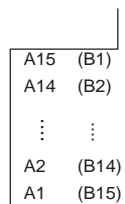


TOUCH PAD

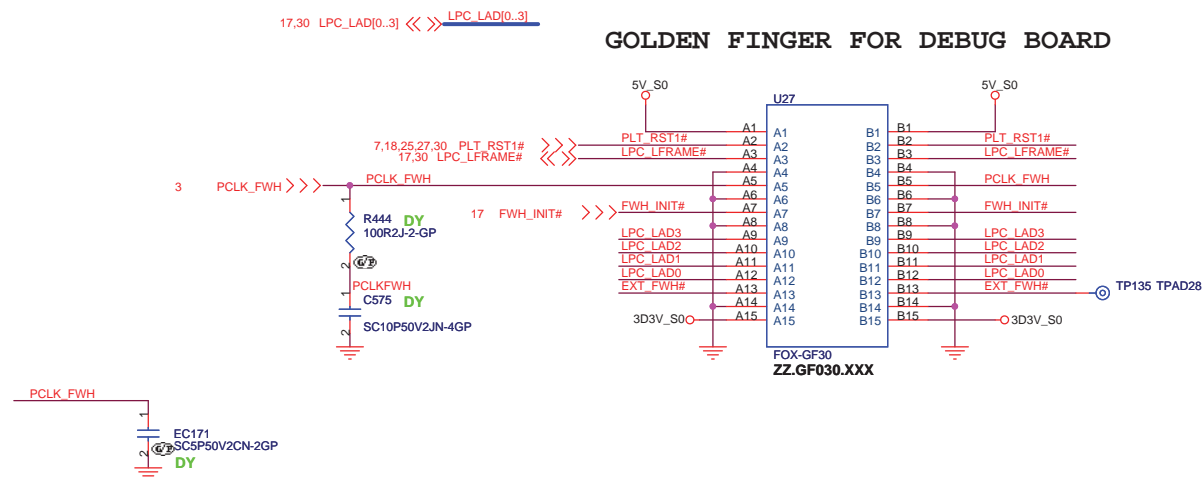




TOP VIEW



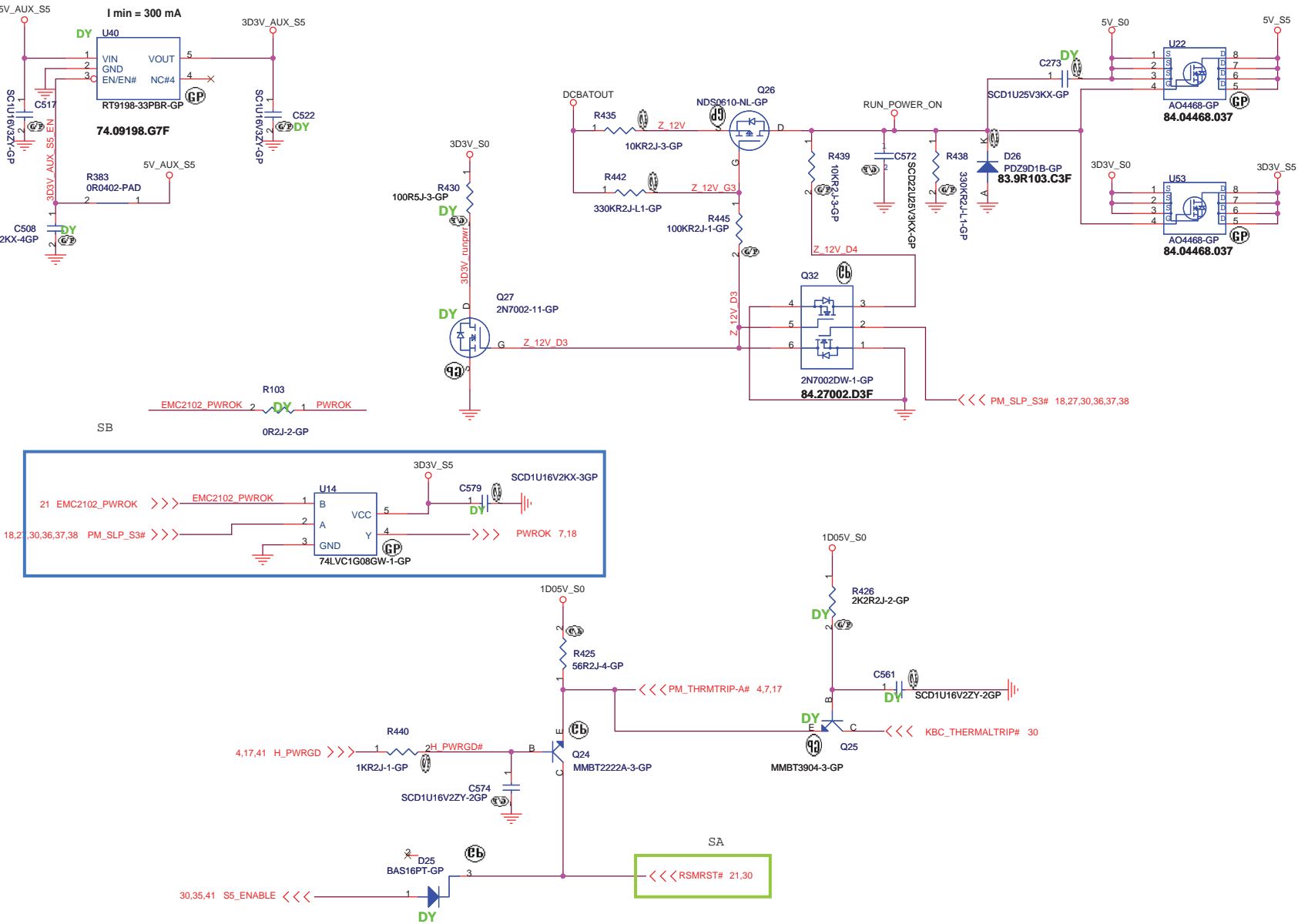
(BOTTOM VIEW)

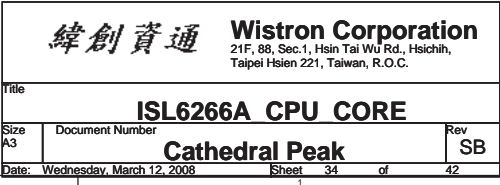


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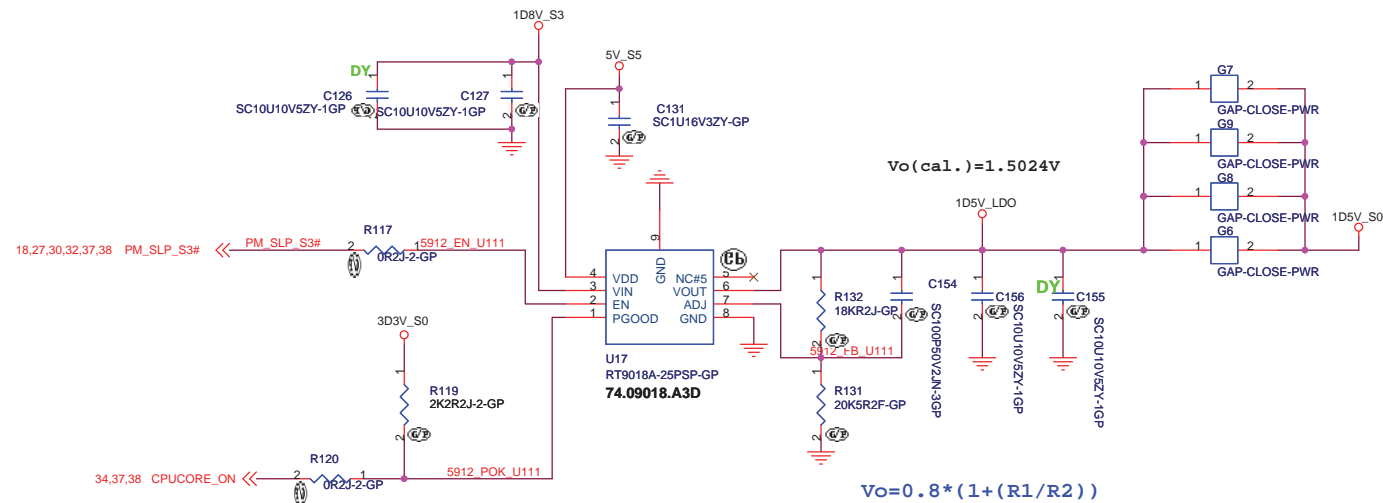
Title			BIOS/GOLDEN FINGER
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Run Power

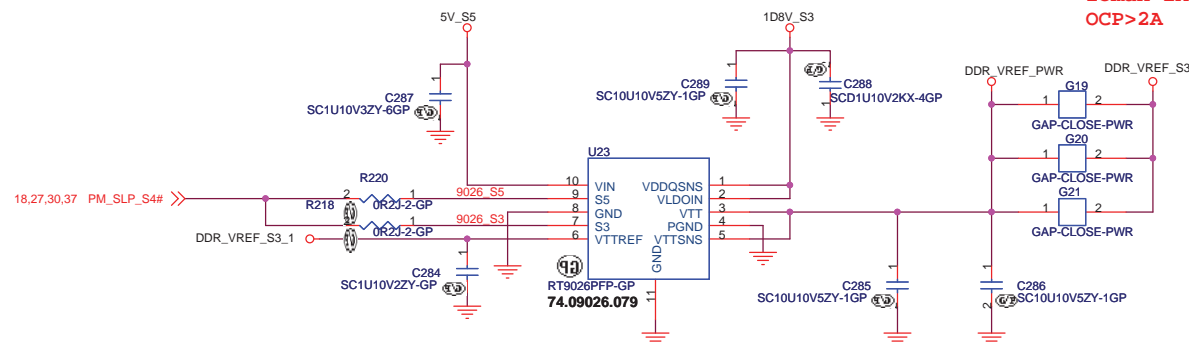


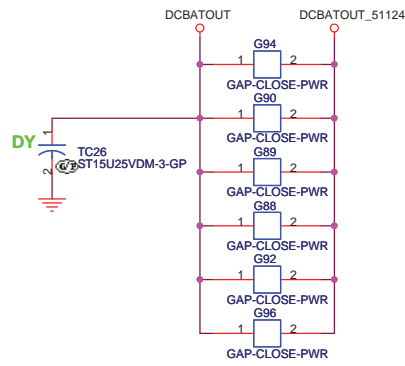


1D5V_S0
I_{omax}=2.5A

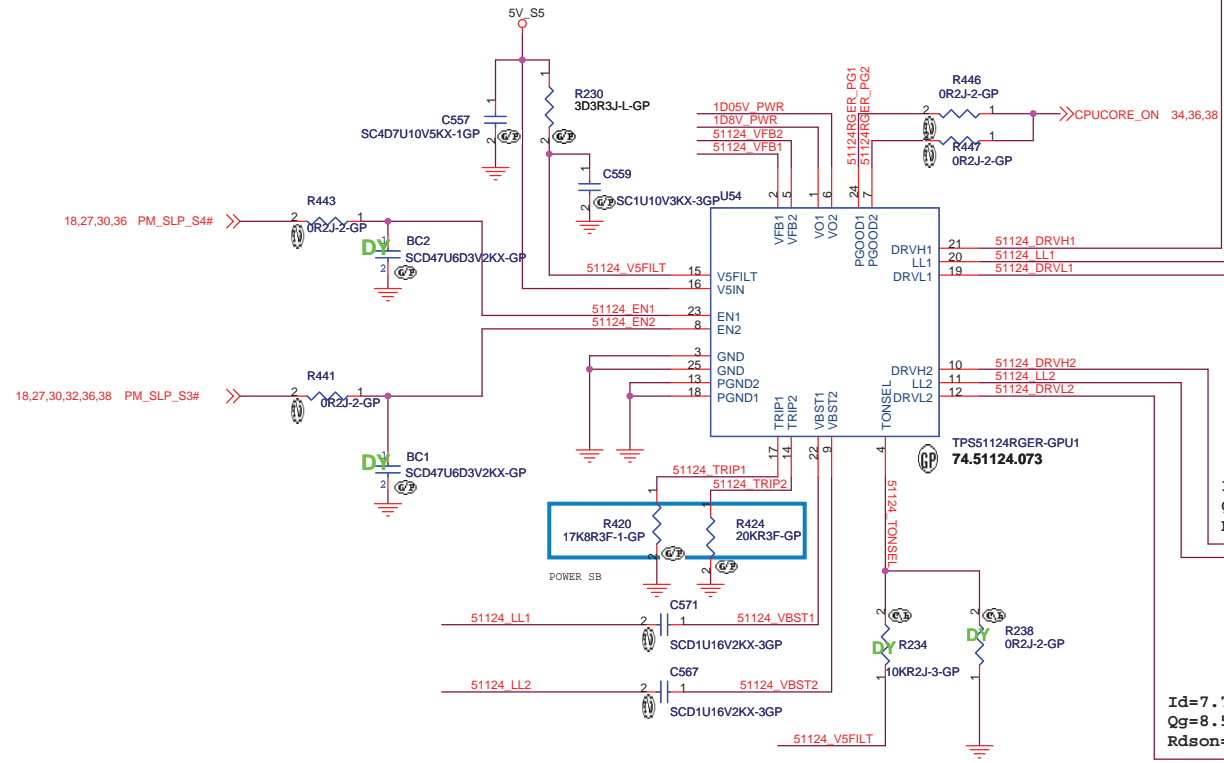


I_{omax}=1A
OCP>2A





$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in}))$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode

<http://hobi-elektronika.net>

緯創資通

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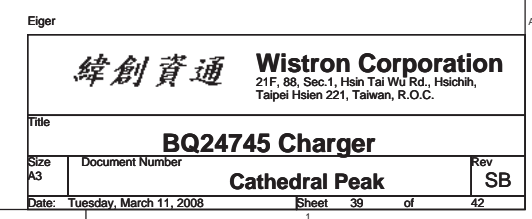
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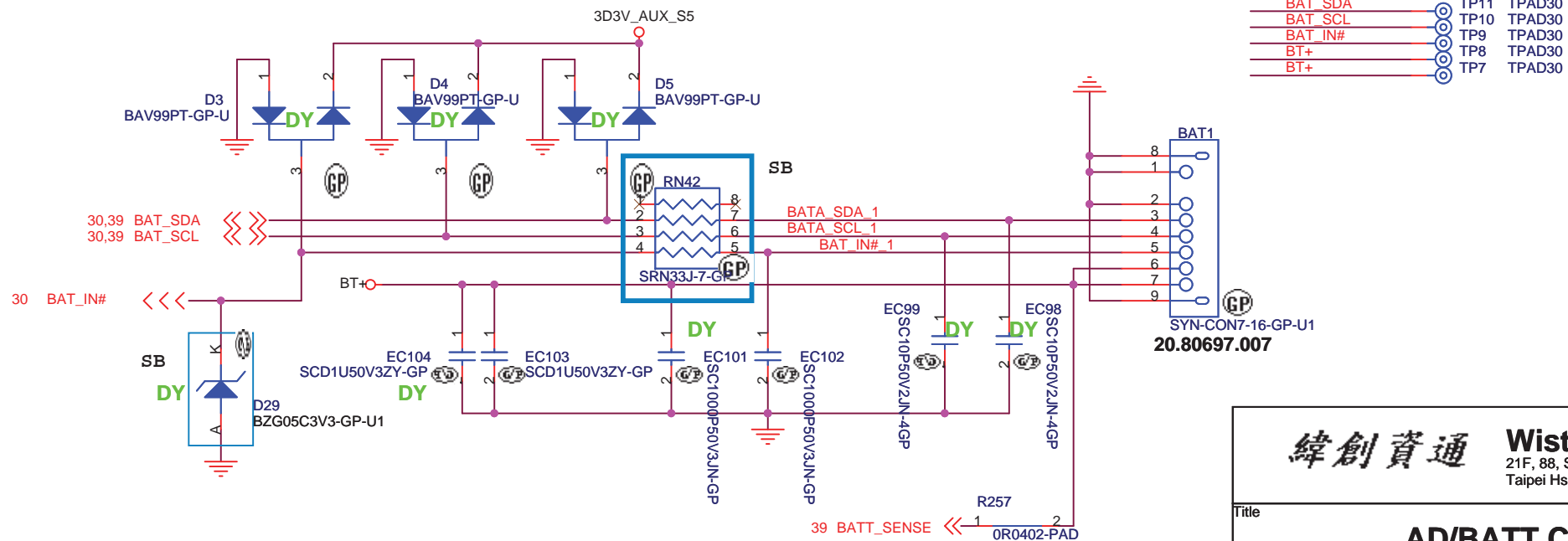
TPS51124 1D8V 1D05V

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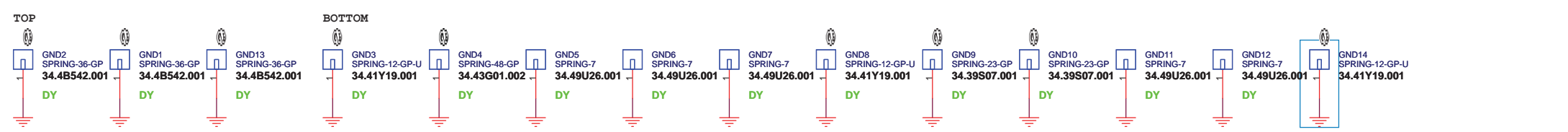
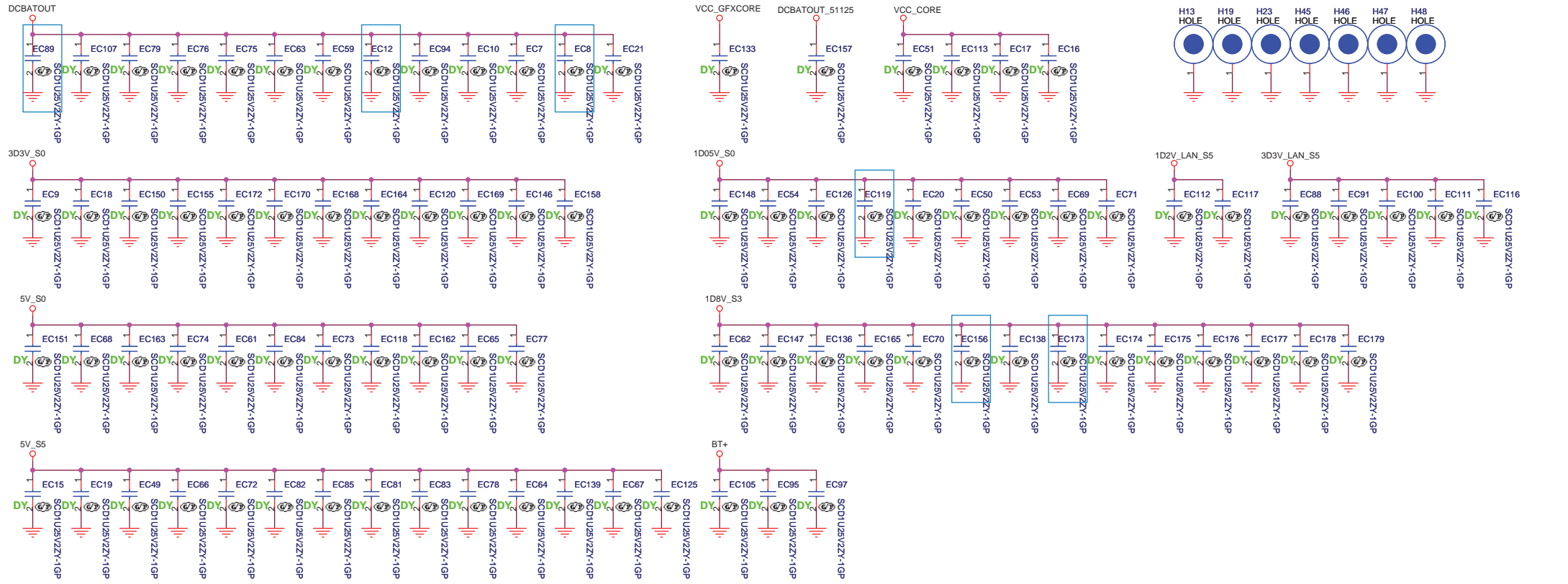
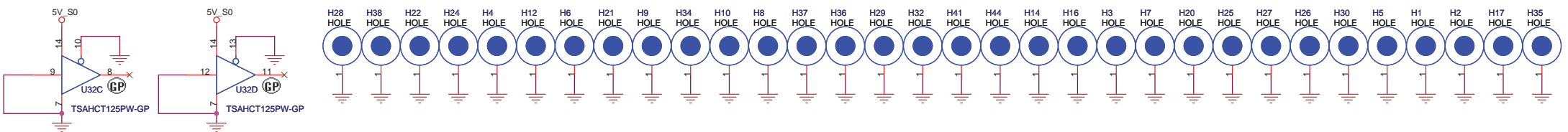


BATTERY CONNECTOR



緯創資通 **Wistron Corporation**
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AD/BATT CONN			
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Check test point

- 3D3V_S0 ○ TP179 TPAD30
- 3D3V_AUX_S5 ○ TP180 TPAD30
- 3D3V_S5 ○ TP181 TPAD30
- 5V_S5 ○ TP182 TPAD30
- 18,30 PM_PWRBTN# <<< TP183 TPAD30
- 4,17,32 H_PWRGD <<< TP184 TPAD30
- 30,32,35 S5_ENABLE <<< TP185 TPAD30
- 4,6 H_CPUURST# <<< TP186 TPAD30

Test Point放在Dimm Door打開可量測處

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緯創資通

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Title		
EMI/Spring/Boss		
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SA to SB
1.No Power.
change KBC to BO (71.03310.A0G)
2.XD Card function fail
Cut CARD1 pin27. connect to R400 pin2
3.leakage
GFX power VDD connect to S0
4.Gain=8db.1.83W R137=16K.R138=30K
5.Int_MIC voice to small
add VREF C577=4.7U
6.Realtek Audio report
change R327=68 ohm.R333=68 ohm.merge to RN68
7.SIV reset
R140=300,R55=100.C44=100p,R398=0,R369=100.C502=100p,R85=300,R162=100.C210=100p,R392=0,
8.SIV Azalia
DY C542
BITCLK rise and fall time fail RN10 change to R453=22ohm(MDC).R452=0ohm(codec)
9.add MINICard power option for customer ask
R454.R455
10.interfere HDD
C390.C401.C419. change 0603 4.7U
11.power team
R38=12K.R47=2.74K .R361=110K.R221=100K.R237=10.7K .R424=20K.R420=17.8K .R227=10.5K
R48=10K.R29=2.2 .R37=2.2 .R401=3.3 .C49=0.1u.add R456.add C580.D8=83.R0203.08F .
TC11 change to 77.C2271.00L
TC9 change to 77.E9071.001 (power ripple)
add R458=1K.R459=1k.R460
12.Oscillation
C30=15p.C23=15P.C537=27p.C538=22p
13.audio S3.S4 resume bobo sound
R143 DY. R187 0ohm pad
14.AC mode have hight frequency noise
R390 DY.R389 0ohm pad
15.ESD issue
BAT_IN# series 33 ohm
RN42 change to 8p4r
add R457.D27.D28.D29.U55.U56.C578.R457.
16.noise
DY C523.TC25 change to 77.C1561.01L
20.LED brightness
R2.R1.R4.R5.R451.R450.R449.R448=56

EMI
1.EC23 ~~EC48.EC134.EC135.EC167.EC121.EC122.EC123.
2.EC89.EC12.EC8.EC119.EC156.EC173.
3.EC174~~~EC179.
4.GND13.GND14.

Merge
1.R313.R314.R315.R319.R320.R149. change to RN59
2.RN6.RN46. change to RN6
3.R341.R343.R344 change to RN46
4.R385 change to 100K merge R382 to RN56
5.RN53.RN56. change to RN53
6.Q20.Q21 change to Q21. Q21.Q23 change to Q21.
7.R367.R368 change to RN60
8.Q16.Q17 change to Q16
9.R262.R264.R268.R277 change to RN61
10.R205.R204.R206 change to RN62
11.RN33.R215 change to RN33
12.R209.R210.R348 change to RN63
13.R280=10K.merge R269 to RN64
14.R109.R112.R111.R290 change to RN65
15.R325.R323 change to RN66
16.R304.R307 change to RN67
17.U14 change to 73.01G08.L04 .add C579
18.R51.R399 vchange to RN69.

0 Ohm change to PAD
R427.R403.R415.R413.R411.R408.R404.R146.R197.R157.R153.R353.R352.R358.R357.R310.R196.R346.R342.R351.
R191.R203.L14.R212.R350.R179.R217.R6.R7.R242.R294.R278.R279.R292.R293.R232.R233.R410.R393.
R416.R250.R251.R248.R249.R246.R247.R244.R245.R129.R127.R376.ER2.R383.R28.R16.R19.R20.R21.
R22.R23.R24.R25.R57.R58.R365.R164.

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Title			
Change List			
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